

Model Name: GA-P81-D3

1.0

SHEET

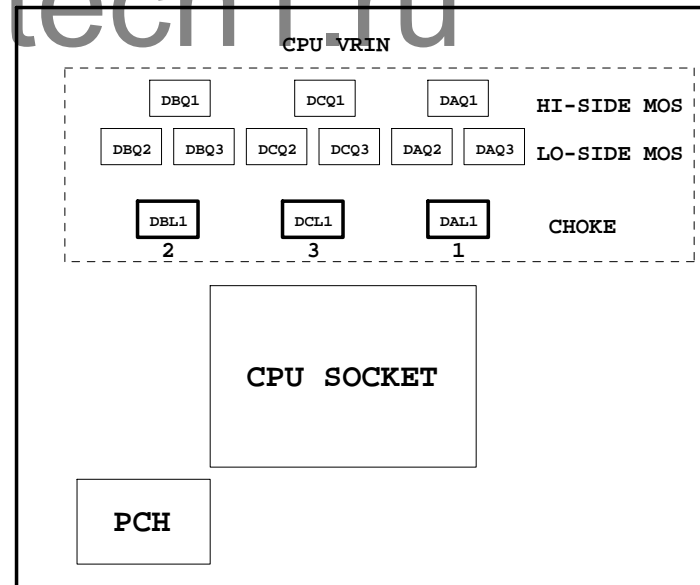
TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1150-A
05	CPU_LGA1150-B
06	CPU_LGA1150-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	PCH_FDI,DMI,USB,PCIE
10	PCH_RGB,CLK BUFFER
11	PCH_HOST,SATA,PCI
12	PCH_GPIO,CTRL,AUDIO
13	PCH_PWR,GND
14	PCI EXPRESS*16 SLOT
15	PCIEX1*2 , PCIEX4 SLOT
16	ITE8892 PCI BRIDGE
17	PCI SLOT 1&2
18	I/O ITE8728
19	COM, -PROHOT, R_USB
20	Dual BIOS / LPT
21	ALC892 CODEC
22	REAR AUDIO JACK
23	VCORE_ ISL95820_1
24	VCORE_ ISL95820_2
25	DDR15V / M3 POWER
26	NCP3933 OVER VOLTAGE
27	DISCRETE POWER

SHEET

TITLE

28	F_PANEL , F_USB2.0/3.0
29	ATX POWER, CLOCK GEN
30	HWM , KB/MS , FAN CTRL
31	Realtek 8111F-VL
32	DVI
33	HDMI
34	TABLE LIST
35	
36	
37	
38	
39	
40	

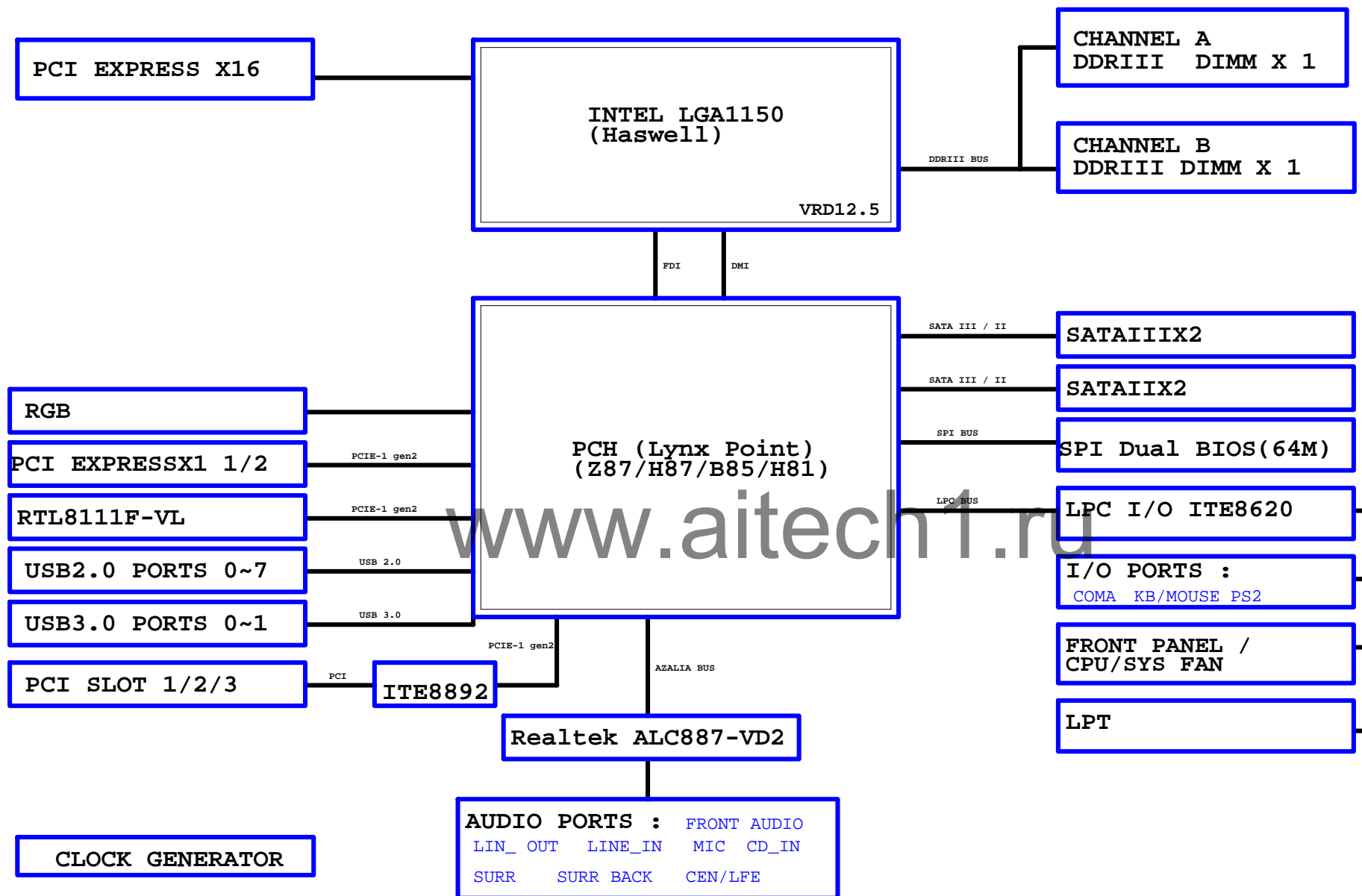


## Component value change history

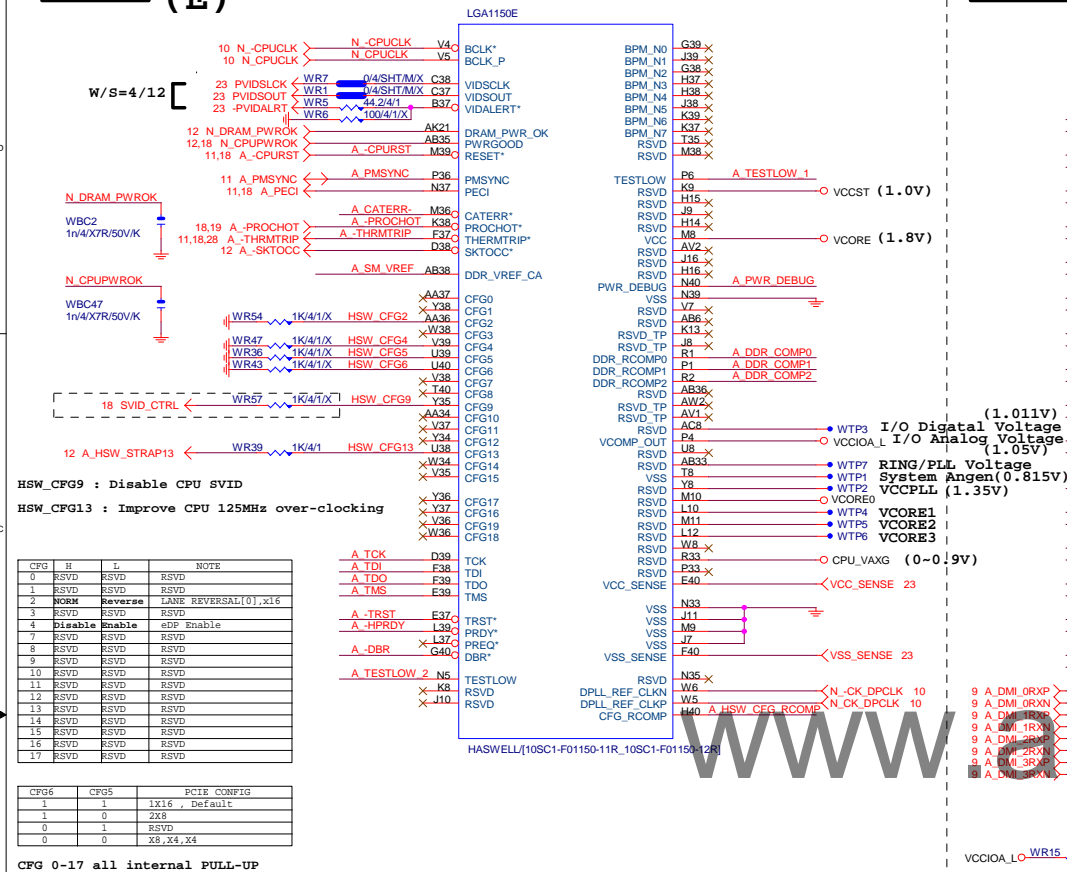
[illegible]

DATE	Change Item	Reason
0.1	1. B85-HD3 Rev1.0 --> H81-HD3 Rev0.1	
0.2	1. 0ohm change to SHORT PAD 2. WBC15-WBC21 Change to "C0805-MASK" 3. Update GBR3/GBR4 footprint 4. U6的NET改走20mil 5. VCC3_DAC gate加粗8mil 6. NCT_POWER加粗至12mil 7. PCH 25MHz周圍走線遠離 8. ESD3 SWAP pin 9. LM324 pin5/7對調	
1.0	1. NX1,NC7,NC8,NR15 第二層切割改至GND層 2. Add NC9-NC12 放在NX1周圍	
1.02	1. Add O_-RSMRST control circuit	
1.03	1.Crystal ( 25MHZ / 32.768KHz) ref GND /width/space 2.CPU fan 0402-----'0603 3.DDR VDDSPD 0402-----'0603/POLU FUSE 4.POWER PAK / 1206 POLY FUSE UPDATE FOOTPRINT 5.UPDTAE Footprint "PCIESLOT-164DN-Q-1"	
1.04	1. Add F_USB20 power short protection	
P81-D3		
1.0	1. H81-D3 REV1.04 --> P81-D3 REV1.0 2. MOS_HS外框移除 , VGA外框移除	

## BLOCK DIAGRAM



LGA1150 (E)



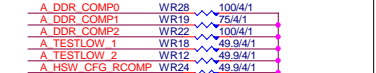
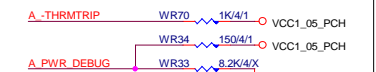
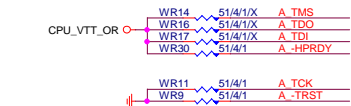
LGA1155 (C)



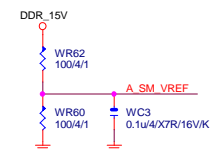
## CPU SVID



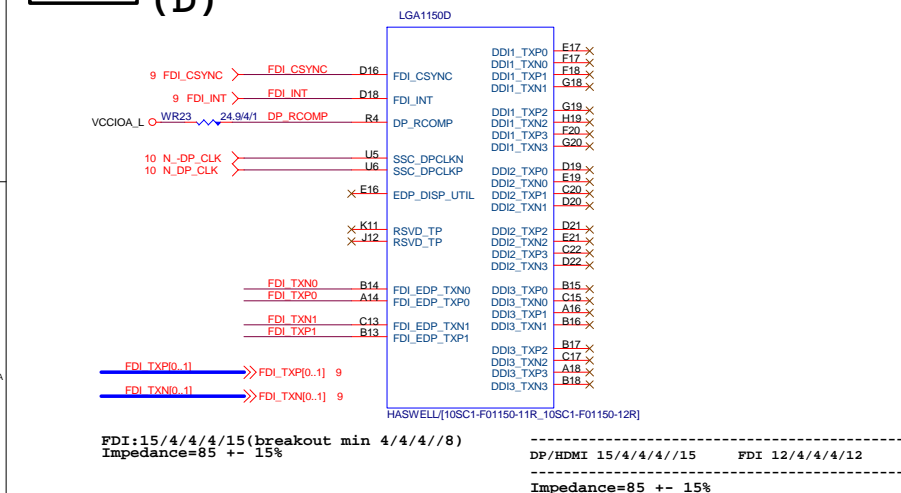
CPU	PU/PD
-----	-------



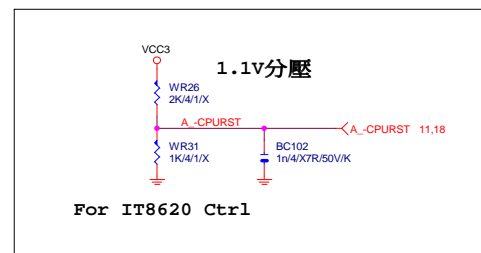
SM REF
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**LGA1150 (D)**



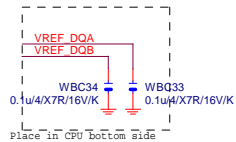
## -CPURST



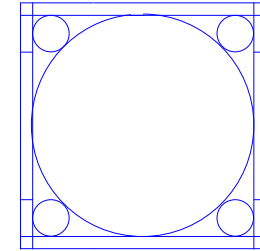
LGA1150A	
MAAA0 AU13	DDR0_MA0
MAAA1 AV16	DDR0_MA1
MAAA2 AU16	DDR0_MA2
MAAA3 AW17	DDR0_MA3
MAAA4 AU17	DDR0_MA4
MAAA5 AW18	DDR0_MA5
MAAA6 AV17	DDR0_MA6
MAAA7 AT18	DDR0_MA7
MAAA8 AU18	DDR0_MA8
MAAA9 AT19	DDR0_MA9
MAAA10 AW11	DDR0_MA10
MAAA11 AV19	DDR0_MA11
MAAA12 AU19	DDR0_MA12
MAAA13 AY10	DDR0_MA13
MAAA14 AT20	DDR0_MA14
MAAA15 AU21	DDR0_MA15
MODT_A0 AW10	DDR0_ODT0
MODT_A1 AY8	DDR0_ODT1
AW9	DDR0_ODT2
AW8	DDR0_ODT3
AW33	DDR0_ECC0
AW33	DDR0_ECC1
AU31	DDR0_ECC2
AW31	DDR0_ECC3
AT33	DDR0_ECC4
AU33	DDR0_ECC5
AT31	DDR0_ECC6
AW31	DDR0_ECC7
SBAA0 SBAA0	DDR0_BA0
SBAA1 SBAA1	DDR0_BA1
SBAA2 SBAA2	DDR0_BA2
CKEA0 CKEA0	DDR0_CKE0
CKEA1 CKEA1	DDR0_CKE1
AW22	DDR0_CKE2
AT23	DDR0_CKE3
AW22	DDR0_CKE4
AW22	DDR0_CKE5
AW22	DDR0_CKE6
AW22	DDR0_CKE7
CSA0 CSA0	DDR0_CS_N0
CSA1 CSA1	DDR0_CS_N1
AW10	DDR0_CS_N2
AW8	DDR0_CS_N3
DCLKA0 DCLKA0	DDR0_CLK_P0
DCLKA0 DCLKA0	DDR0_CLK_N0
DCLKA1 DCLKA1	DDR0_CLK_P1
DCLKA1 DCLKA1	DDR0_CLK_N1
AW14	DDR0_CLK_P2
AW14	DDR0_CLK_N2
AW13	DDR0_CLK_P3
AW13	DDR0_CLK_N3
AW12	RSVD
SRASA SRASA	DDR0_RAS*
SWEA SWEA	DDR0_WE*
AW20	RSVD
AW27C	RSVD
SCASA SCASA	DDR0_CAS*
WR61	DDR_RESET
D4/SH/TMX	
WC4	
0.1u/4/X7R/16V/K/X	

HASWELL[10SC1-F01150-11R\_10SC1-F01150-12R]

LGA1150B	
MAAB0 AL19	DDR1_MA0
MAAB1 AK23	DDR1_MA1
MAAB2 AM22	DDR1_MA2
MAAB3 AM23	DDR1_MA3
MAAB4 AP23	DDR1_MA4
MAAB5 AL23	DDR1_MA5
MAAB6 AY24	DDR1_MA6
MAAB7 AV25	DDR1_MA7
MAAB8 AU26	DDR1_MA8
MAAB9 AV25	DDR1_MA9
MAAB10 AP18	DDR1_MA10
MAAB11 AY25	DDR1_MA11
MAAB12 AV26	DDR1_MA12
MAAB13 AR15	DDR1_MA13
MAAB14 AV27	DDR1_MA14
MAAB15 AY28	DDR1_MA15
MODT_B0 AM17	DDR1_ODT0
MODT_B1 AL16	DDR1_ODT1
AM16	DDR1_ODT2
AK15	DDR1_ODT3
AM26	DDR1_ECC0
AM25	DDR1_ECC1
AP25	DDR1_ECC2
AP26	DDR1_ECC3
AL26	DDR1_ECC4
AL25	DDR1_ECC5
AR26	DDR1_ECC6
AR25	DDR1_ECC7
SBAB0 SBAB0	DDR1_BA0
SBAB1 SBAB1	DDR1_BA1
SBAB2 SBAB2	DDR1_BA2
CKEB0 CKEB0	DDR1_CKE0
CKEB1 CKEB1	DDR1_CKE1
AW29	DDR1_CKE2
AW29	DDR1_CKE3
CSB0 CSB0	DDR1_CS_N0
CSB1 CSB1	DDR1_CS_N1
AM15	DDR1_CS_N2
AM17	DDR1_CS_N3
AL15	DDR1_CLK_P0
AM20	DDR1_CLK_N0
AM21	DDR1_CLK_P1
AP22	DDR1_CLK_N1
AP21	DDR1_CLK_P2
AN20	DDR1_CLK_N2
AN21	DDR1_CLK_P3
AP19	DDR1_CLK_N3
AP20	DDR1_CAS*
AP16C	RSVD
AL20	DDR1_RAS*
AM18C	DDR1_WE*
AK16C	DDR1_DQ0
AB39	DDR_VREF_DQ0
AB40	DDR_VREF_DQ1



HASWELL[10SC1-F01150-11R\_10SC1-F01150-12R]

LGA1150  
ILM\_BP/1156/CSP/[12KRC-0F0001-52R\_12KRC-0F0001-51R]

DDR BUS

MODT_A[0..1]	MODT_A0..1
MODT_B[0..1]	MODT_B0..1
MDA[0..63]	MDA0..63
MDB[0..63]	MDB0..63
DQSA[0..7]	DQSA0..7
DQSA[0..7]	DQSA0..7
MAAA[0..15]	MAAA0..15
MAAB[0..15]	MAAB0..15
DQSB[0..7]	DQSB0..7
DQSB[0..7]	DQSB0..7

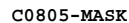
Gigabyte Technology

Title		CPU LGA1150-B	
Size	Document Number	GA-P81-D3	
Custom			Rev 1.0
Date:	Wednesday, March 05, 2014	Sheet	5 of 34

(F, J)



(x18)



(x9)



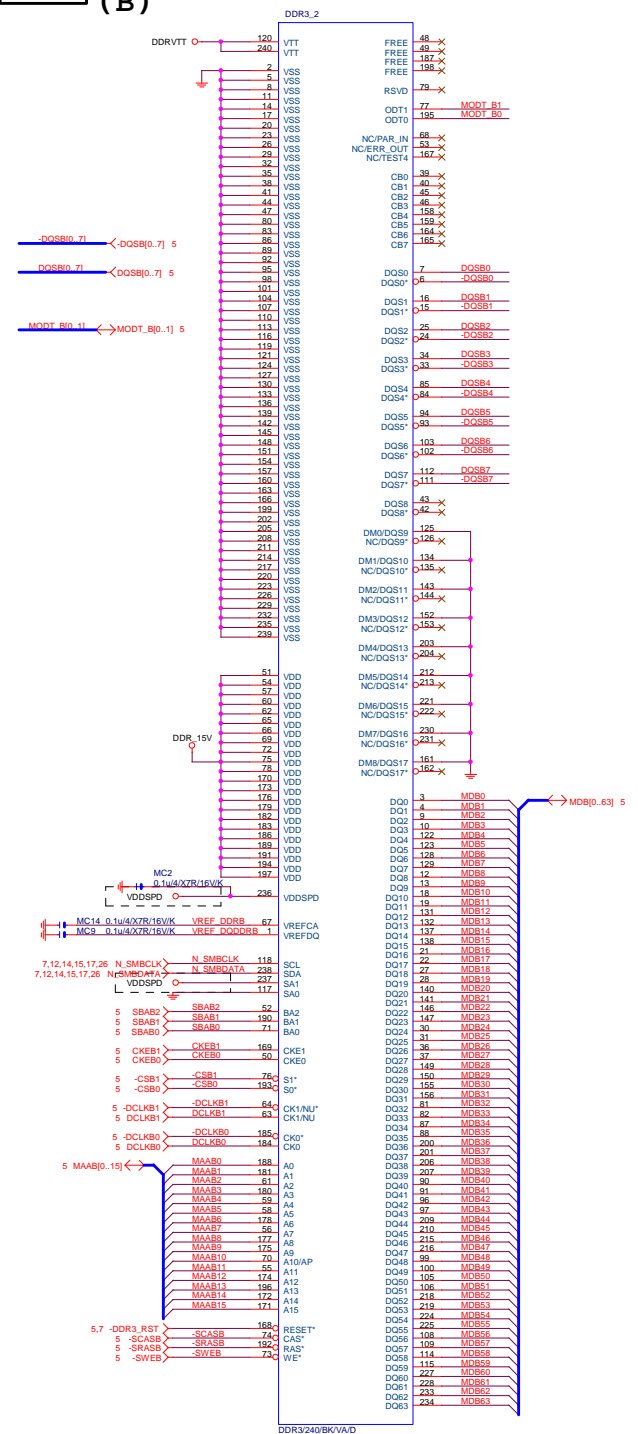
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Size	Document Number	Rev	
Custom	GA-P81-D3	1.0	
Date:	Wednesday, March 05, 2014	Sheet	6 of 34



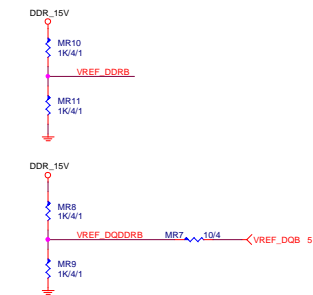


DDR3

(B)



DDR3 VREF



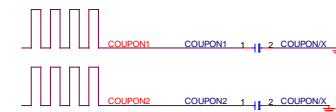
DDR3 1066,1333,1600MHZ BANDWIDTH

DDR3 1066MHZ  
DDR3 clock=533MHZ  
DDR3 single channel bandwidth=533x2x8Byte=8.5GB/s  
DDR3 dual channel bandwidth=533x2x2x8Byte=17GB/s

DDR3 1333MHZ  
DDR3 clock=667MHZ  
DDR3 single channel bandwidth=10.6GB/s  
DDR3 dual channel bandwidth=21GB/s

DDR3 1600MHZ  
DDR3 clock=800MHZ  
DDR3 single channel bandwidth=12.8GB/s  
DDR3 dual channel bandwidth=25.6GB/s

COUPON



CPU

DTMM1 (黑色) CHA

DTMM2 (黑色) CHB

Gigabyte Technology

Title			DDR3 CHANNEL B
Size			Document Number
Custom			GA-P81-D3
Date			Rev 1.0
Sheet			8 of 34



(B)

USB2.0 : 12/5/7/5/12 (breakout min 8/4/4/4/8)  
Impedance=85 +- 15%



**放靠近** Device & PCI-E Slot

H81/S/[10HB1-030H81-19R]

PCH PCIe .DMI 15/4/4/4//15 Impedance=85 +- 15%

usb2.0 12/5/7/5/12

Impedance=85 +- 15%

(J)



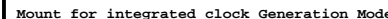
(F)



H81:12/13 N\.



USB3.0:20/5/7/5/20 (breakout min  
8/4/4/4/8) ; ONLY 3 VIAS  
Impedance=85 +- 17.5%  
Back Panel < 10000 MILS  
Front Panel < 6000 MILS



PCH H/S

# LOW COST PCH HEATSINK



HEAT SINK/N-BG/GBT MK/Z87/KWOG/I12SP2-S04208-61R 12SP2-S04208-62R 12SP2-S04208-63R

NEW H81 MODEL  
Footprint: BGAHSINK-75;  
3mm孔徑

USB	TABLE
-----	-------

```
OC[3:0]# for Device 29 (ports 0-7)
OC[7:4]# for Device 26 (ports 8-13)
```

USB OC# Configure

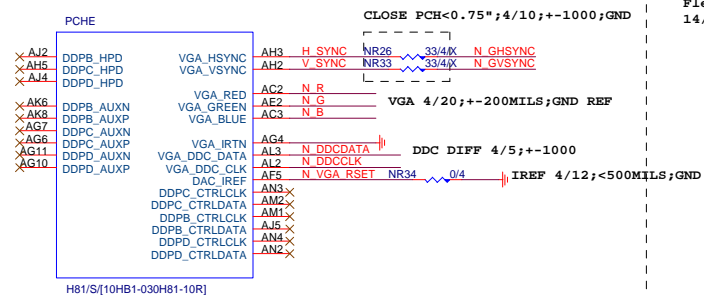
## Gigabyte Technology

Title	Author	Year	Journal	Volume	Issue	Page
1. The Effect of Temperature on the Rate of Reaction	John Doe	2018	Journal of Chemical Education	95	3	456-462
2. Kinetics of the Reaction Between Hydrogen Peroxide and Potassium Iodide	Jane Smith	2017	Journal of Chemical Education	94	2	321-328
3. The Effect of Concentration on the Rate of Reaction	Michael Brown	2016	Journal of Chemical Education	93	1	123-130
4. The Effect of Surface Area on the Rate of Reaction	Sarah White	2015	Journal of Chemical Education	92	4	567-574
5. The Effect of Catalyst on the Rate of Reaction	David Black	2014	Journal of Chemical Education	91	5	678-685

GA-P81-D3

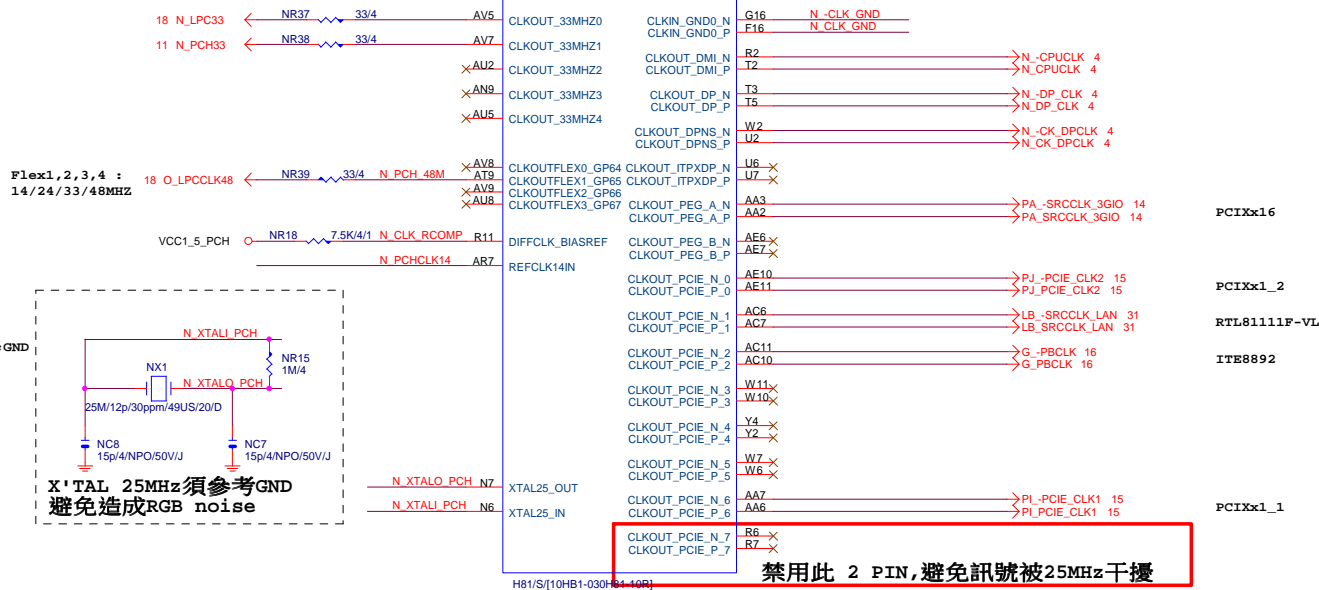
Date: Wednesday, March 05, 2014 Sheet 9 of 3

**PCH (E)**



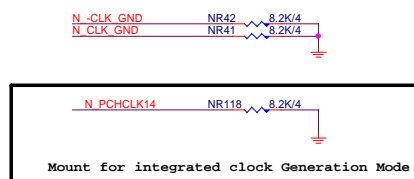
VGA_DISABLE
R,G,B NC OR GND
IRTN / IREF GND
VGA_HSYNC, VGA_VSYNC, DDC_CLK, DDC_DATA NC
POWER VCCADAC(AF2), VCCADACBG(AE1) GND

**PCH (G)**

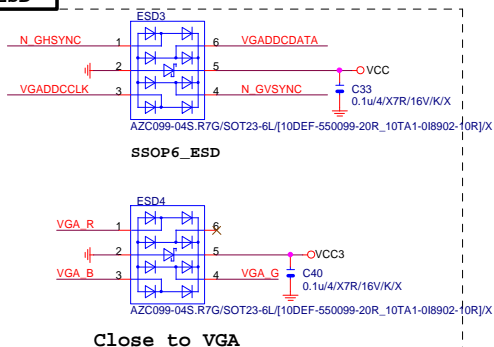


Differential Clock:18/4/6/4/18  
Impedance=90 +- 15%

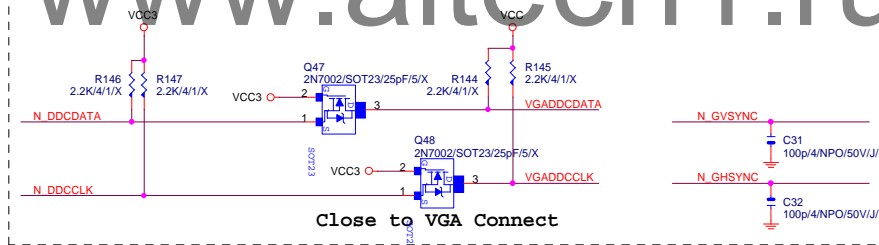
PCH CLK PD
------------



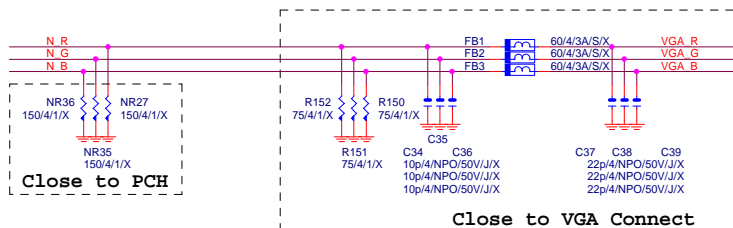
## VGA ESD



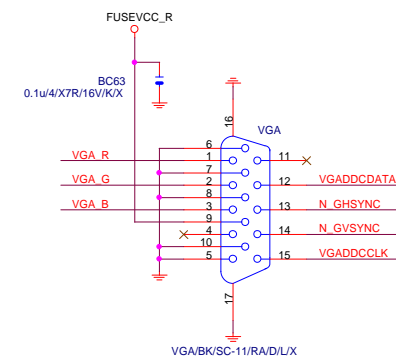
## VGA DDC



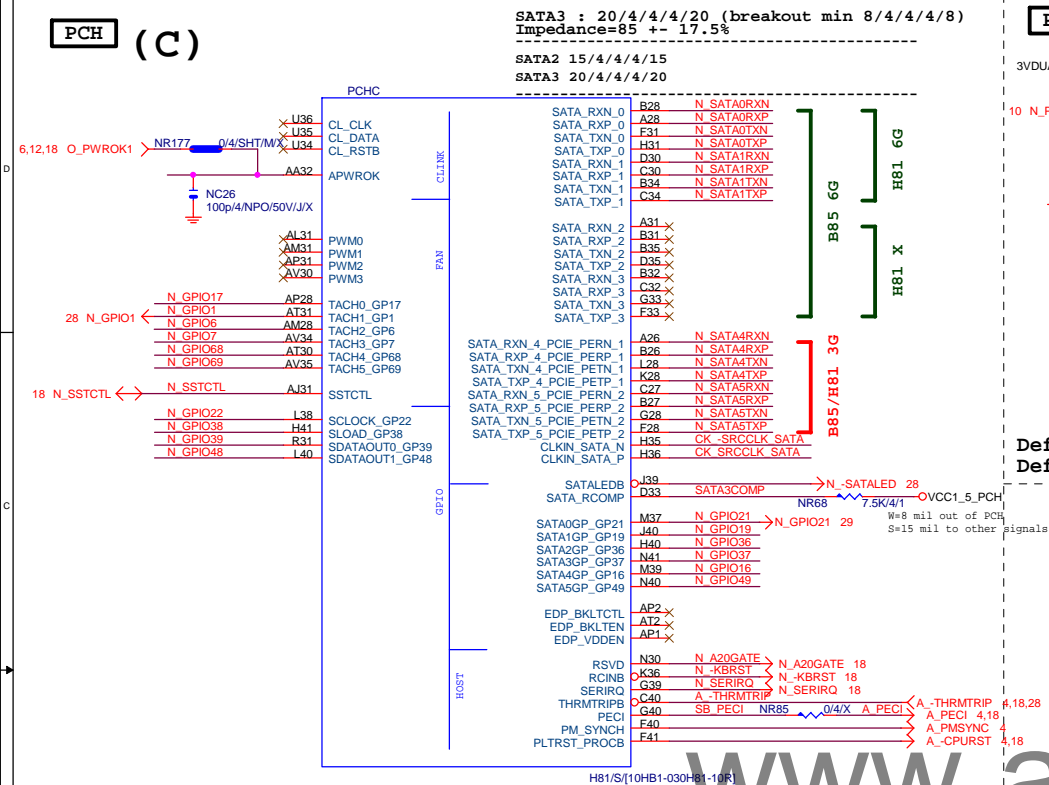
## VGA DDC



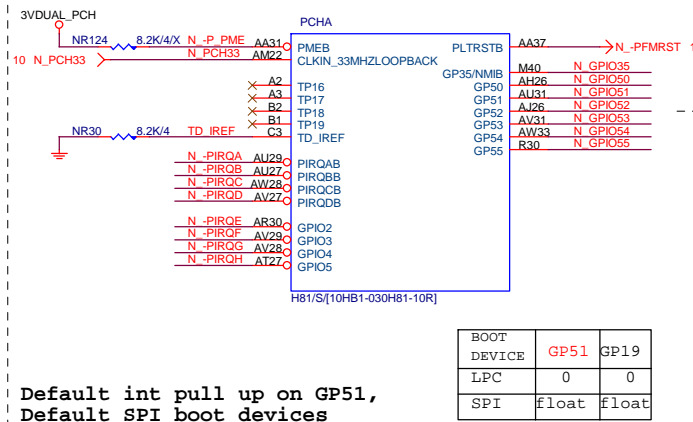
## VGA CONNECTOR



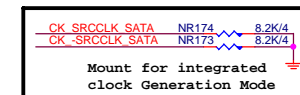
**PCH (C)**



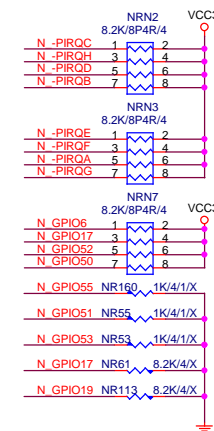
**PCH (A)**



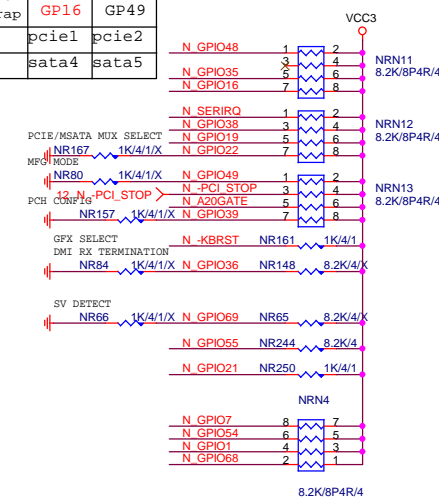
PCH CLK PD



PCH	PU/PD
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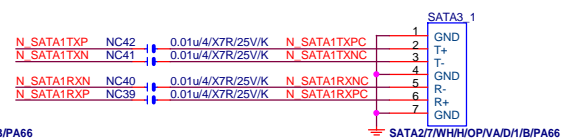
soft strap	GP16	GP49
0	pcie1	pcie2
1	sata4	sata5



## SATA CONNECTOR



WHITE CONNECTOR



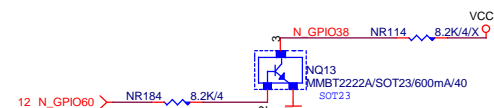
## WHITE CONNECTOR

[Z87/H87] all SATA3  
SATA3(From Z87) - 黑色  
SATA3(From Marvell) - 灰色  
[B85] SATA2+SATA3  
SATA2(From B85) - 黑色  
SATA3(From B85) - 白色

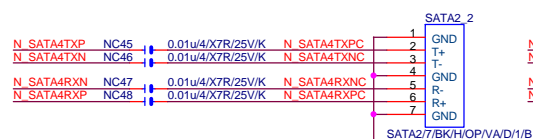
GPIO38 Ctrl

MFG Mode

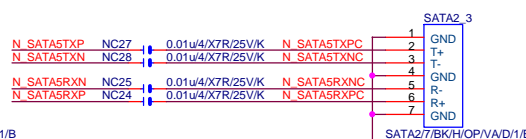
```
N_GPIO38 : Lo --> Enable
           Hi --> Disable
```



```
** Z87/H87 Port 4&5 SATA3.0
** B85 Port 4&5 SATA2.0
```

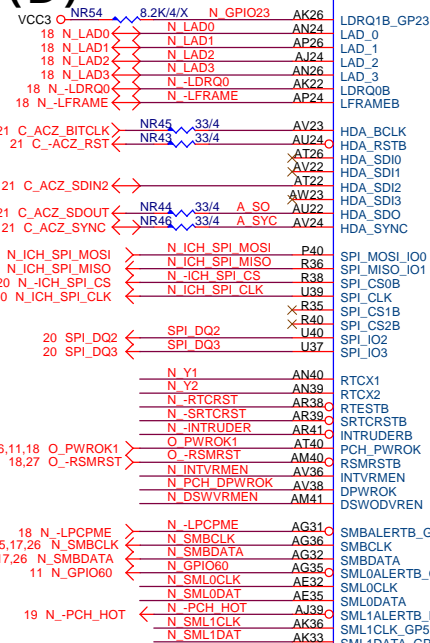


BLACK CONNECTOR

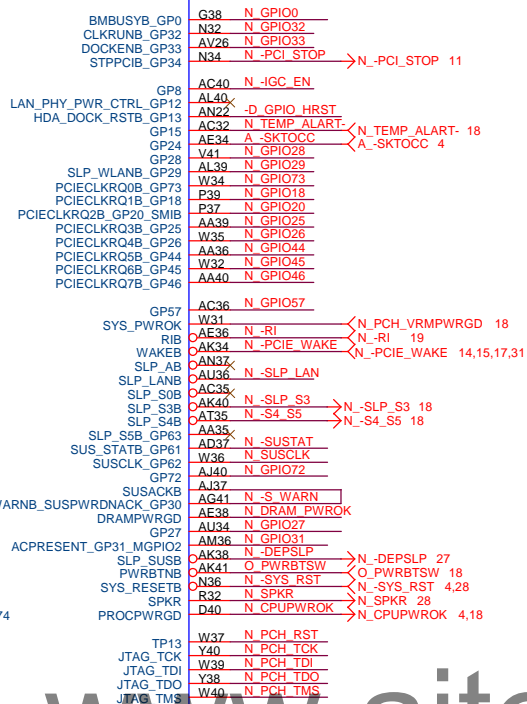
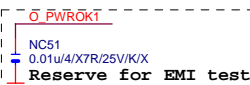


BLACK CONNECTOR

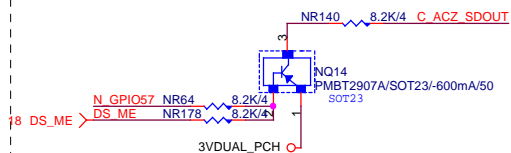
(D)



H81/S/[10HB1-030H81-10R]



```
C_ACZ_SDOUT : HI --> ME Enable
              Lo --> ME Disable
HI:disable ME and override SPI Flash Access
Permissions
```



**For IT8620 Ctrl**

NR139	8.2K/4/X	N_GPIO46	1	2	NRN99 8.2K/8P4/4
NR155	8.2K/4/X	N_GPIO45	5	6	
NR103	8.2K/4/X	N_GPIO44	4	6	
		N_GPIO57	7	8	
	A -SKTOCC		1	2	NRN10 8.2K/8P4/4
	N_TEMP_ALARM-		3	4	
	N -RI		5	6	
GP8:Low to enable			X	8	
PCH clock chip					
NR106	1K/4/1	N -IGC_EN	NR105	8.2K/4/X	
NR153	1K/4/1/X	N_SUSCLK	NR154	8.2K/4/X	
SUSCLK:Low to OD					
PLL VR					
GP28:Lo disable					
VRM ,Hi enable					
VRM					
	N -S_WARN	NR129	8.2K/4		3VDUAL_PCH ○
	N_GPIO27	NR60	8.2K/4		
	N_GPIO31	NR72	8.2K/4		
	N -SLP_LAN	NR73	8.2K/4/X		
	N_GPIO72	NR100	8.2K/4		
	N -POE_WAKE	NR65	1K/4/1		
	N_GPIO29	NR96	1K/4/1/X		
					VCC3
NR145	8.2K/4/X	N_GPIO20	NR109	8.2K/4	
		N_GPIO0	NR115	8.2K/4	
		N -SYS_RST	NR164	8.2K/4	
		N_GPIO32	NR162	8.2K/4/X	
NR48	8.2K/4/X	N_GPIO33	NR49	8.2K/4	
					3VDUAL ○
	N_PCH_RST	NR172	200k/4/1		
	N_PCH_TDI	NR170	200k/4/1		
	N_PCH_TDO	NR141	200k/4/1		
	N_PCH_TMS	NR169	200k/4/1		
	N_PCH_TCK	NR87	200k/4/1/X		
	N_PCH_RST	NR143	1K/4/1/X		
	N_PCH_TDI	NR171	100k/4/1		
	N_PCH_TDO	NR168	100k/4/1		
	N_PCH_TMS	NR142	100k/4/1		
	N_PCH_TCK	NR108	51k/4/1		
	GPIO18	NR79	8.2K/4		
	GPIO73	NR134	8.2K/4		
	GPIO26	NR107	8.2K/4		
	GPIO25	NR137	8.2K/4		
	-SYS_RST	NC58	1n/4k/X	R50V/K	
	DRAM_PWROK	NC59	1n/4k/X	R50V/K	

[illegible]

**BATTERY-DUAL-4**

**RB 必須放在BAT外**

N\_INTRUDER NR74 1M/4 <N\_RTCVDD 13,28

N\_SRTCRST NR77 20K/4/1 <N\_RTCVDD 13,28

NC19 1u4/X5R/6.3V/K

NC20 1u4/X5R/6.3V/K

NR15 1u4/X5R/6.3V/K

NR67 390K/4 N\_INTVRMEN

NR78 20K/4/1 N\_RTCRST

NR90 390K/4 N\_DSWVRMEN

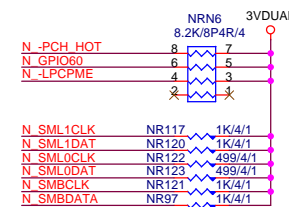
N\_RTCVDD 13,28

N\_VBAT 18

CLR\_CMOS

PH1\*2/BK/2.54/VA/D

N\_INTERMEN: Integrated 1.05V SUS VRM Enable



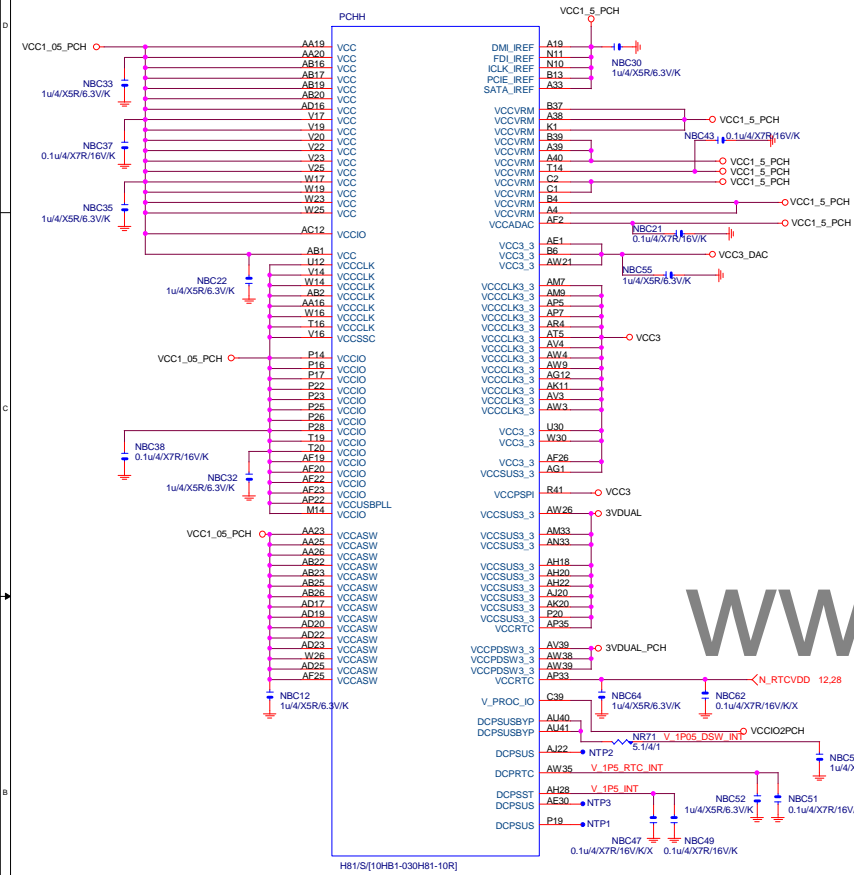
## Gigabyte Technology

## PCH GPIO , CTRL , AUDIO

**GA-P81-D3**

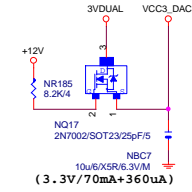
Title			
PCH GPIO , CTRL , AUDIO			
Size	Document Number	Rev	
Custom	GA-P81-D3	1.0	
Date:	Wednesday, March 05, 2014	Sheet	12 of 34

PCH (H)

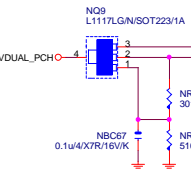


VCC3\_DAC

CLOSE北橋(注意震盪水波紋)



3VDUAL\_PCH

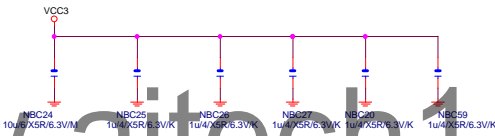


SHT\_PWR

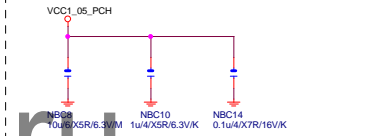


CAP

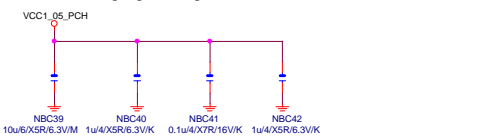
(3.3V) (X6)



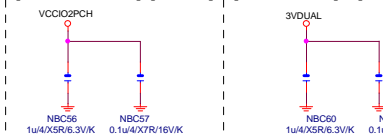
(1.05V) (X5)



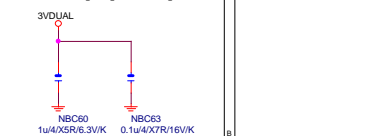
(1.05V) (X6)



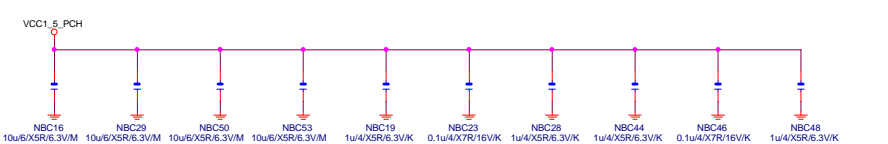
(1.05V) (X2)



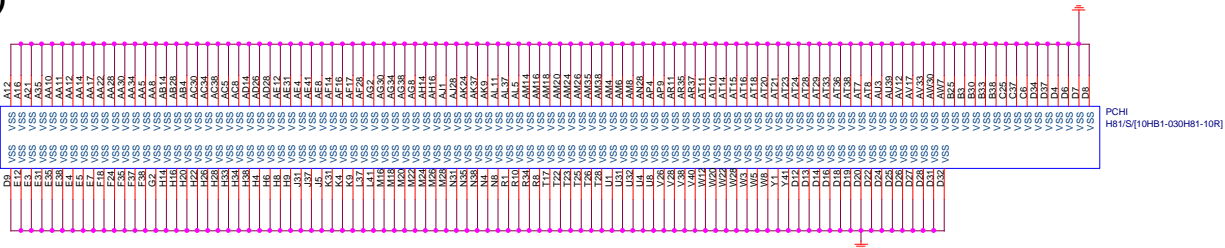
(3.3V) (X2)



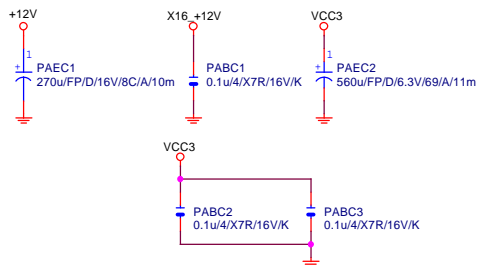
(1.5V) (X10)



PCH (I)

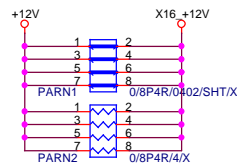


PCIEX16 CAP
-------------



PCIEX16	PROTECT	SHT
---------	---------	-----

```
+12 protect
short-wire test
```



PCIEX16	AC	CAP
---------	----	-----

PA EXP TXP0	PAC5	0.22u4/X5R6.3V/K	PA EXP TXP0 C
PA EXP TXN0	PAC4	0.22u4/X5R6.3V/K	PA EXP TXN0 C
PA EXP TXP1	PAC6	0.22u4/X5R6.3V/K	PA EXP TXP1 C
PA EXP TXN1	PAC7	0.22u4/X5R6.3V/K	PA EXP TXN1 C
PA EXP TXP2	PAC8	0.22u4/X5R6.3V/K	PA EXP TXP2 C
PA EXP TXN2	PAC9	0.22u4/X5R6.3V/K	PA EXP TXN2 C
PA EXP TXP3	PAC10	0.22u4/X5R6.3V/K	PA EXP TXP3 C
PA EXP TXN3	PAC11	0.22u4/X5R6.3V/K	PA EXP TXN3 C
PA EXP TXP4	PAC12	0.22u4/X5R6.3V/K	PA EXP TXP4 C
PA EXP TXN4	PAC13	0.22u4/X5R6.3V/K	PA EXP TXN4 C
PA EXP TXP5	PAC14	0.22u4/X5R6.3V/K	PA EXP TXP5 C
PA EXP TXN5	PAC15	0.22u4/X5R6.3V/K	PA EXP TXN5 C
PA EXP TXP6	PAC16	0.22u4/X5R6.3V/K	PA EXP TXP6 C
PA EXP TXN6	PAC17	0.22u4/X5R6.3V/K	PA EXP TXN6 C
PA EXP TXP7	PAC18	0.22u4/X5R6.3V/K	PA EXP TXP7 C
PA EXP TXN7	PAC19	0.22u4/X5R6.3V/K	PA EXP TXN7 C
PA EXP TXP8	PAC20	0.22u4/X5R6.3V/K	PA EXP TXP8 C
PA EXP TXN8	PAC21	0.22u4/X5R6.3V/K	PA EXP TXN8 C
PA EXP TXP9	PAC22	0.22u4/X5R6.3V/K	PA EXP TXP9 C
PA EXP TXN9	PAC23	0.22u4/X5R6.3V/K	PA EXP TXN9 C
PA EXP TXP10	PAC24	0.22u4/X5R6.3V/K	PA EXP TXP10 C
PA EXP TXN10	PAC25	0.22u4/X5R6.3V/K	PA EXP TXN10 C
PA EXP TXP11	PAC26	0.22u4/X5R6.3V/K	PA EXP TXP11 C
PA EXP TXN11	PAC27	0.22u4/X5R6.3V/K	PA EXP TXN11 C
PA EXP TXP12	PAC28	0.22u4/X5R6.3V/K	PA EXP TXP12 C
PA EXP TXN12	PAC29	0.22u4/X5R6.3V/K	PA EXP TXN12 C
PA EXP TXP13	PAC30	0.22u4/X5R6.3V/K	PA EXP TXP13 C
PA EXP TXN13	PAC31	0.22u4/X5R6.3V/K	PA EXP TXN13 C
PA EXP TXP14	PAC32	0.22u4/X5R6.3V/K	PA EXP TXP14 C
PA EXP TXN14	PAC33	0.22u4/X5R6.3V/K	PA EXP TXN14 C
PA EXP TXP15	PAC34	0.22u4/X5R6.3V/K	PA EXP TXP15 C
PA EXP TXN15	PAC35	0.22u4/X5R6.3V/K	PA EXP TXN15 C

PCI-E REV:1.1--&gt; 2.5GHZ

PCE-E X1(單向) BANDWIDTH=2.5GHz\*(8b/10b)=2Gb/s=250MB/s

PCE-E X1(雙向) BANDWIDTH=2.5GHz\*(8b/10b)X2=4Gb/s=500MB/s

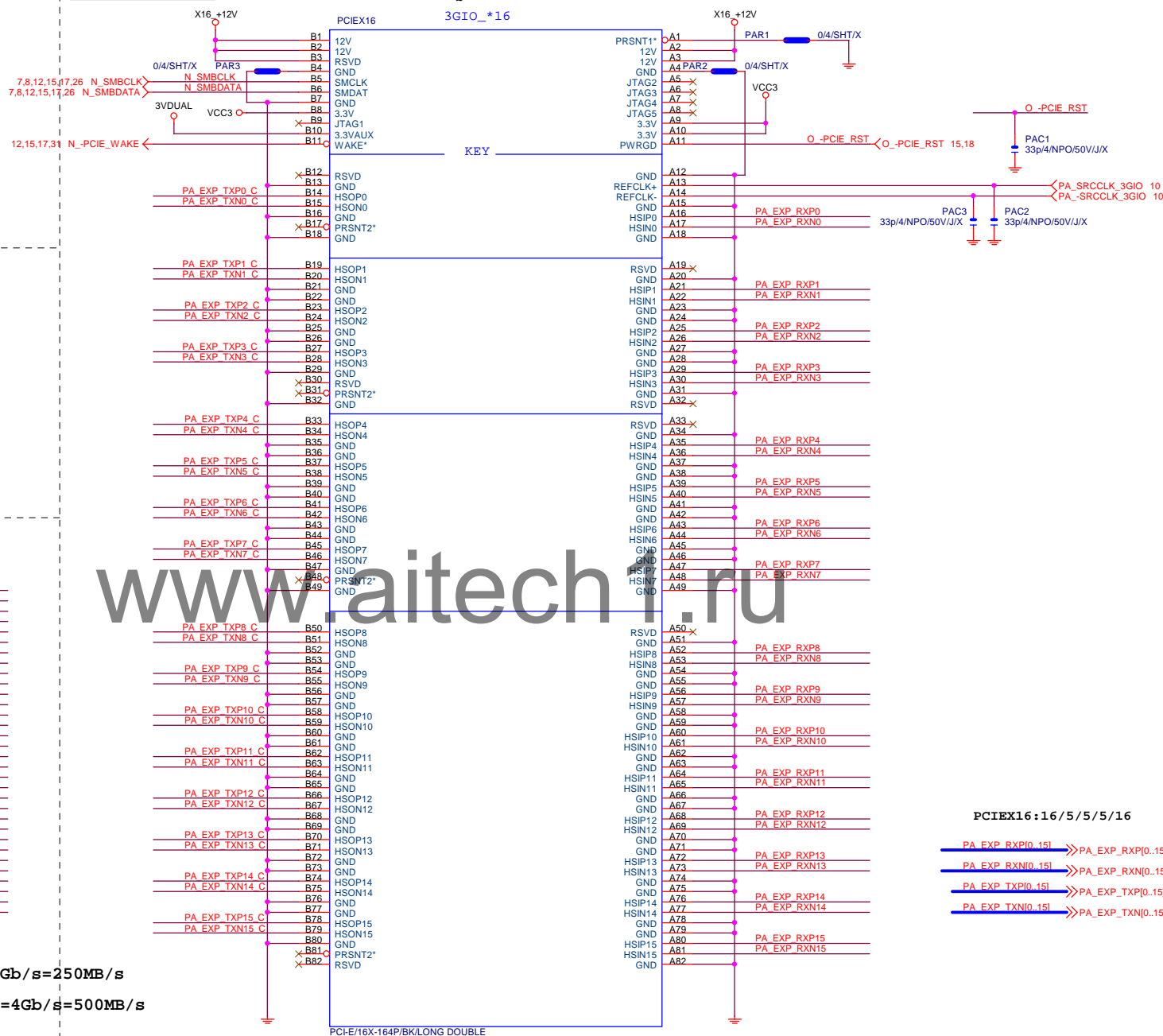
PCE-E X16(單向) BANDWIDTH=2.5GHz\*(8b/10b)X16=32Gb/s=4GB/s

PCE-E X16(雙向) BANDWIDTH=2.5GHz\*(8b/10b)X16X2=64Gb/s=8GB/s

PCI-E REV:2.0--&gt; 5GHZ

## PCIEX16 SLOT

## PCIESLOT-164DN-Q



PCIEX16:16/5/5/5/16

PA EXP RXP[0..15]     $\gg$  PA EXP RXP[0..15] 4

PA EXP RXN[0..15]     $\Rightarrow$  PA EXP RXN[0..15] A

PA EXP TXP[0..15]    \ PA EXP TXP[0..15] 4

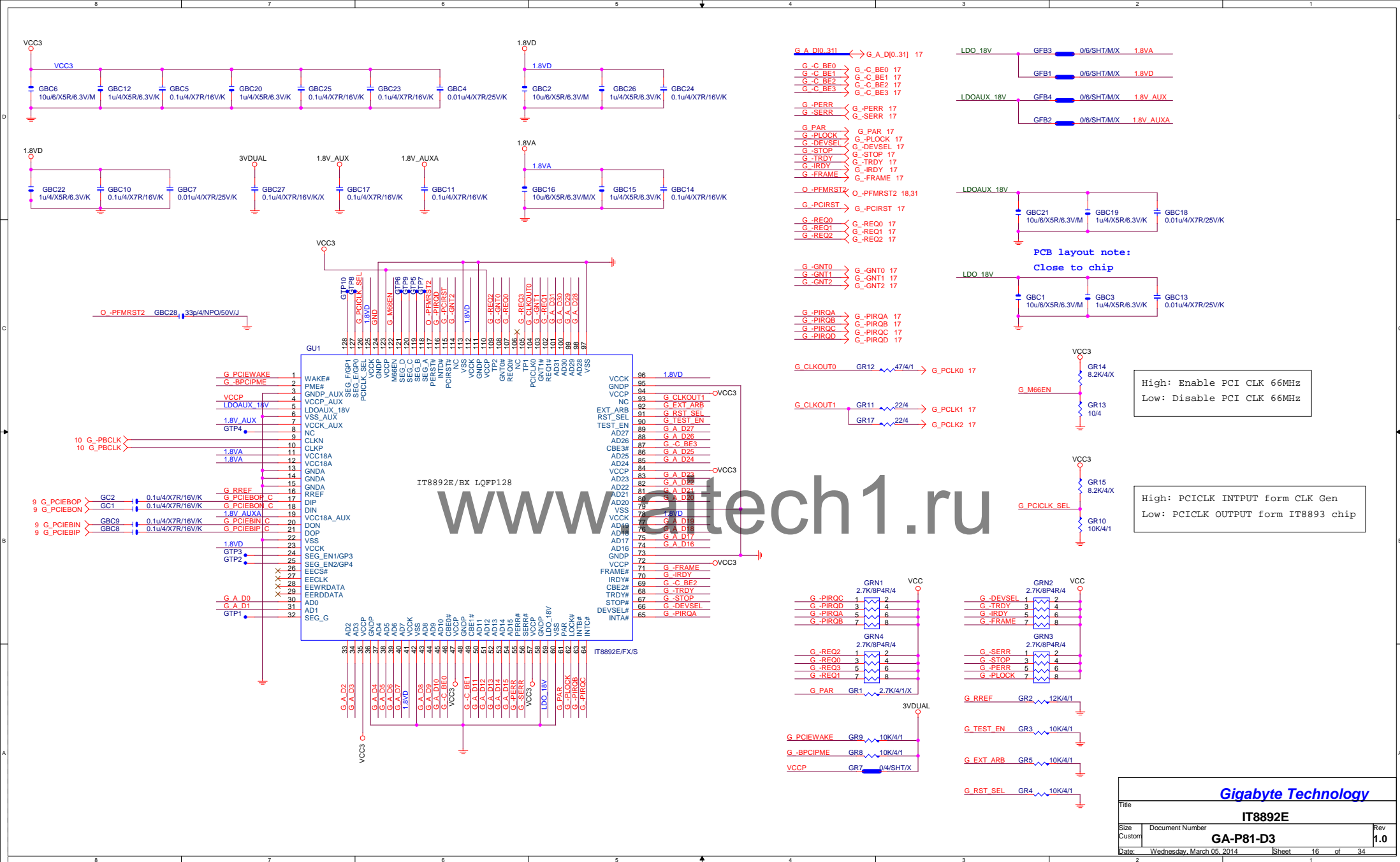
PA EXP TXN[0..15] \ PA EXP TXN[0..15]

<b>Gigabyte Technology</b>			
Title <b>PCI EXPRESS * 16</b>			
Size Custom	Document Number <b>GA-P81-D3</b>		Rev <b>1</b>
Date:	Wednesday, March 05, 2014	Sheet	14 of 34

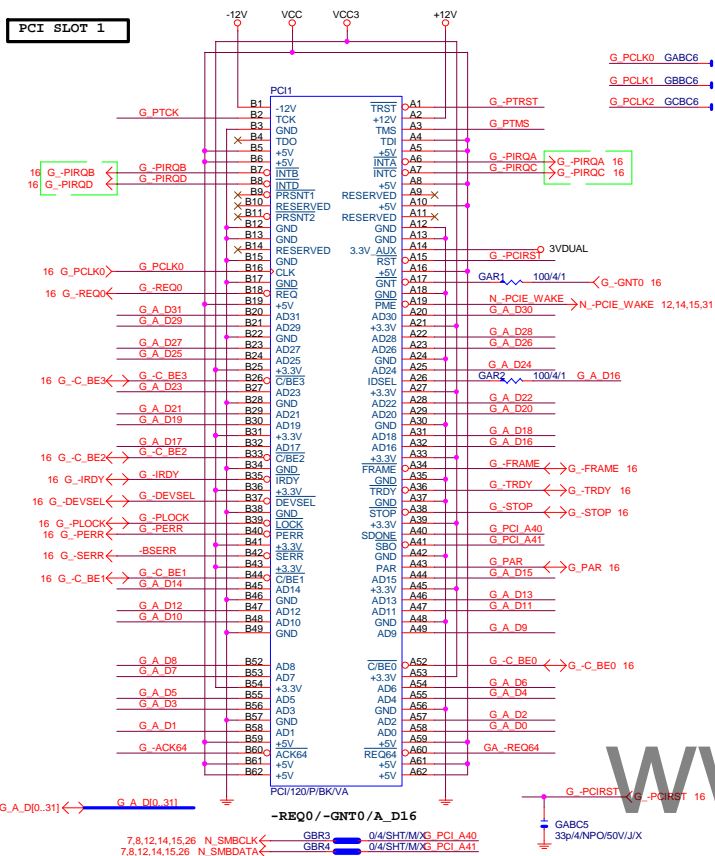




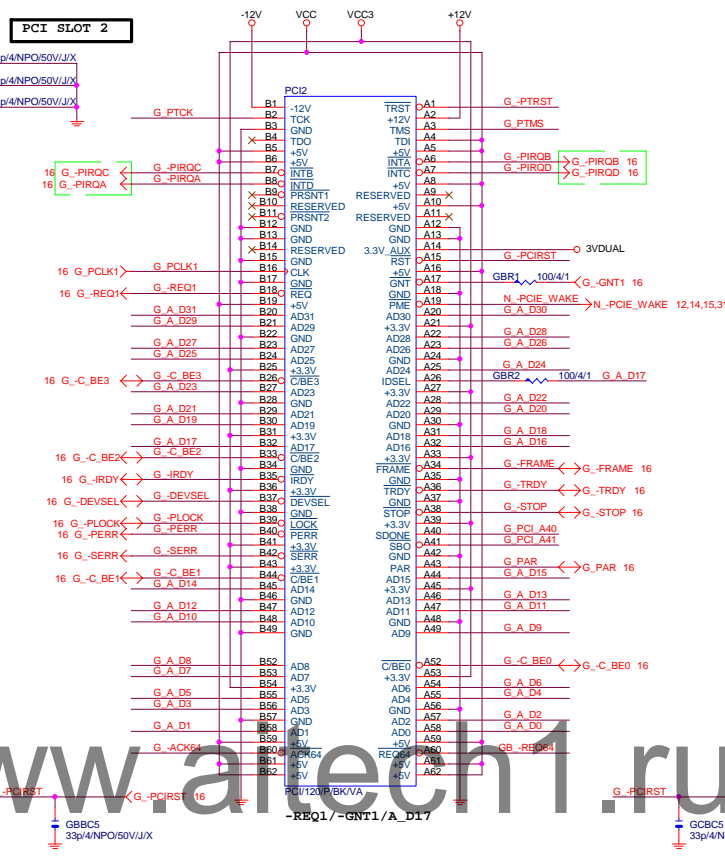




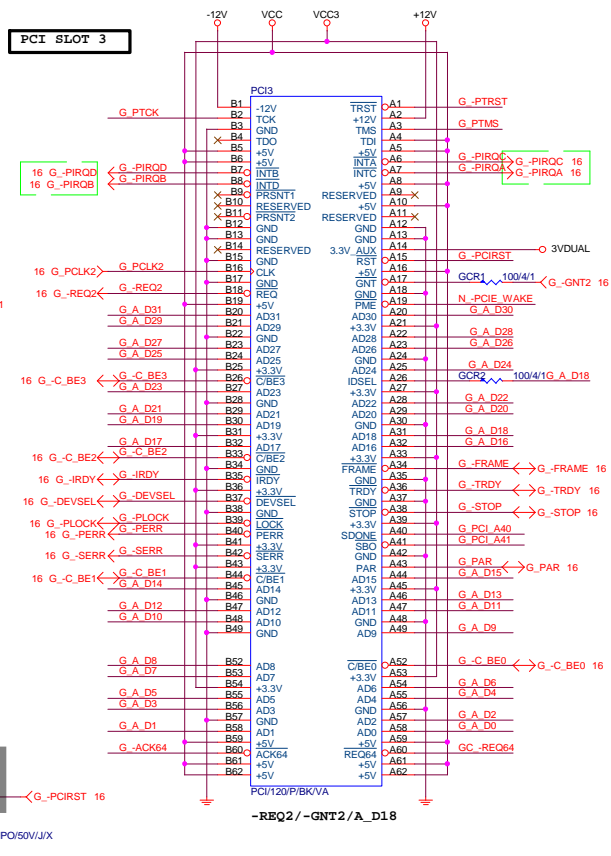
# PCI SLOT 1



# PCI SLOT 2

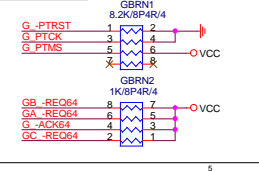


# PCI SLOT 3

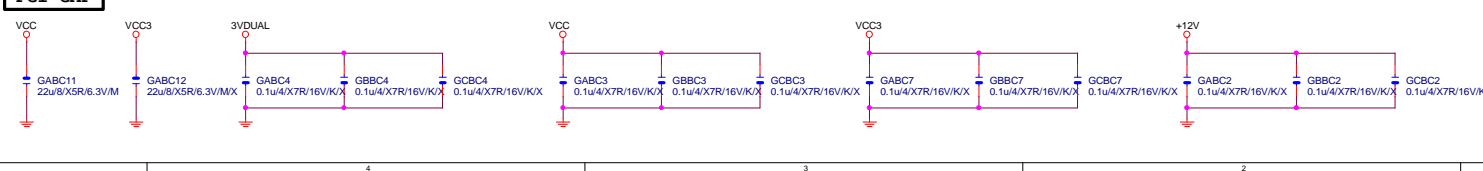


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# PCI PU

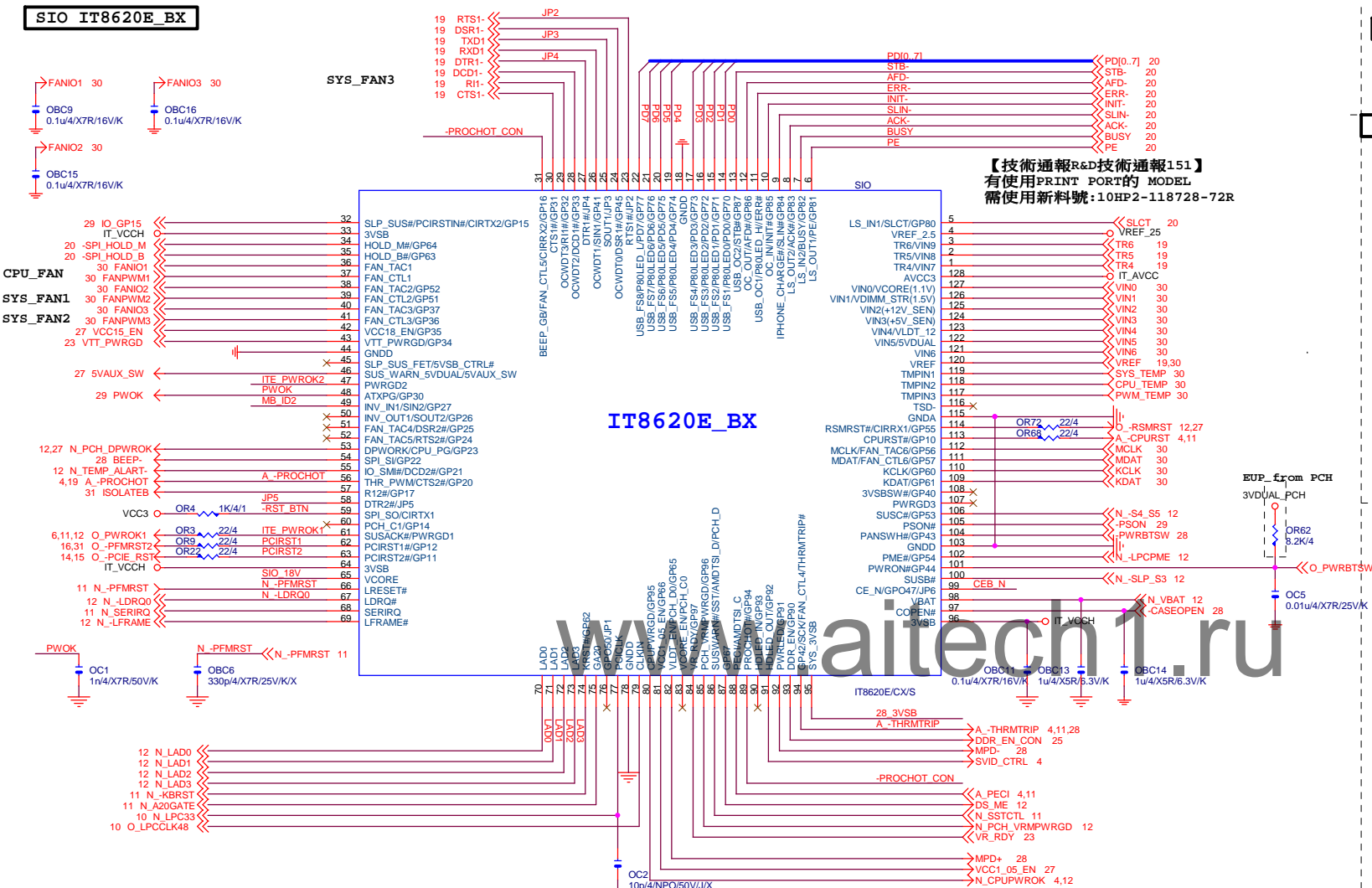


# PCI CAP

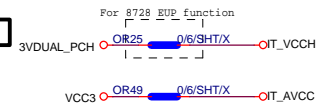


<b>GIGABYTE™</b>			
Title <b>PCI SLOT 1&amp;2</b>			
Size	Document Number	Rev	
Custom	<b>GA-P81-D3</b>	<b>1.0</b>	
Date:	Wednesday, March 05, 2014	Sheet	17 of 34

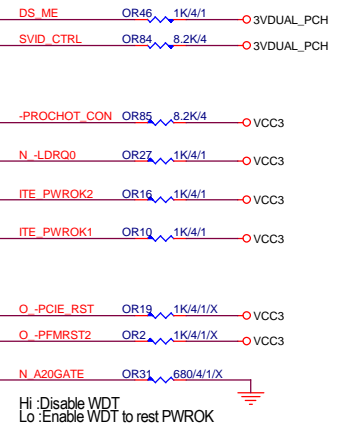
## SIO IT8620E\_BX



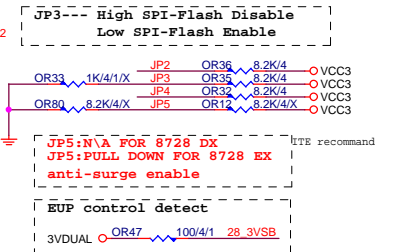
## PWR SHT



## SIO PU



## SIO STRAP

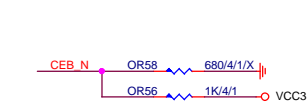


JP4	1	k8 power sequency function is Disable
JP4	0	k8 power sequency function is Enable
JP3	1 1	The default value of EC Index 63h/6Bh/73h is 80h.
JP3	1 0	The default value of EC Index 63h/6Bh/73h is FFh.
JP5	0 1	The default value of EC Index 63h/6Bh/73h is 00h.
JP5	0 0	The default value of EC Index 63h/6Bh/73h is 40h.

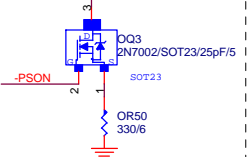
## IT8620E GPIO問題匯整

PIN 50	GP26---
PIN 90/91	第一次接上POWER時會拉 LO
PIN 108	DEFAULT為HDLDED FUNCTION, GP93 BYPASS TO GP92
PIN 111/112	GP40--- POWER ON 時會拉 LO
PIN 111/112	MOUSE 跟FAN6 FUNCTION 擇一使用,不然會互相干擾

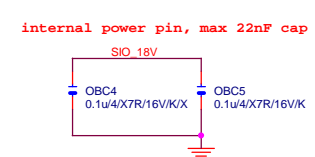
## DUAL BIOS OPT STRAP



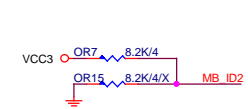
## Power leakage



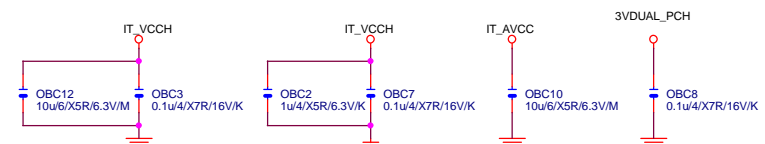
## SIO\_18V



## MB ID



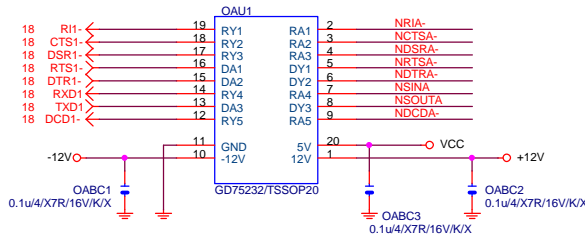
## SIO CAP



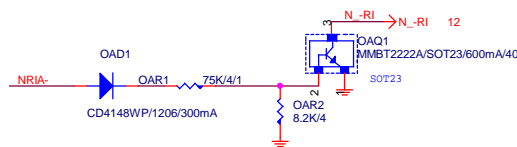
## Gigabyte Technology

Title		
ITE 8728 LPC IO		
Size	Document Number	Rev
Custom	GA-P81-D3	1.0
Date:	Monday, March 24, 2014	Sheet 18 of 34

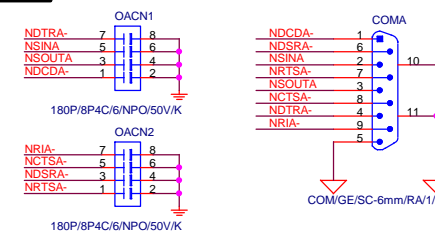
## COMA



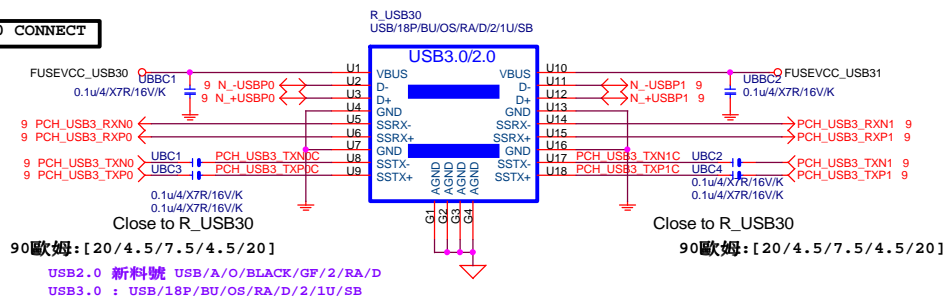
## COM RI



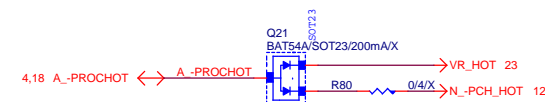
## COM BUFFER



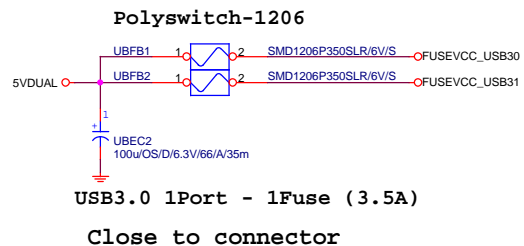
## R\_USB30 CONNECT



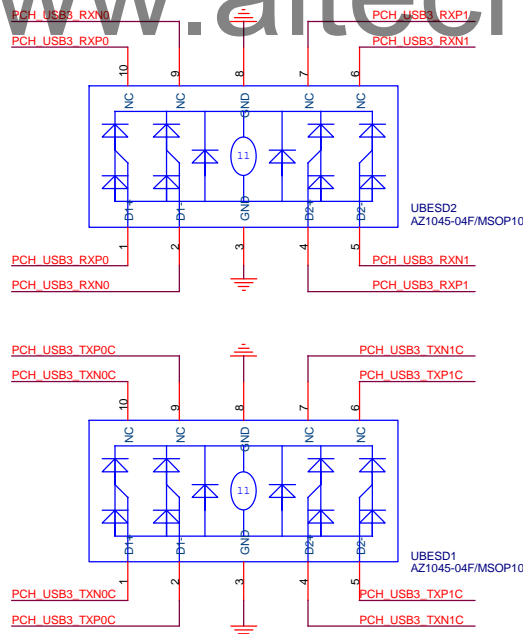
## -PROHOT



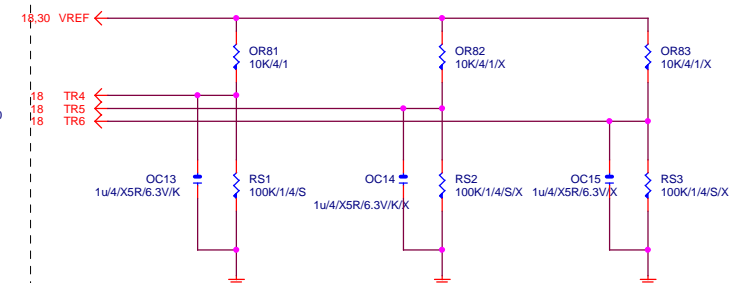
## USB30 PWR



## USB30 ESD PROTECT

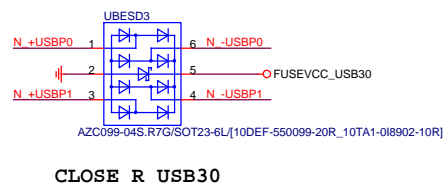


## PROHOT



RS1 close DBQ1、  
RS2 close DDQ1、  
RS3 close DAQ1、  
Others close SIO

## USB20 ESD PROTECT



Gigabyte Technology

Title		COM & PROHOT/Dynamic O.C.	
Size	Document Number	Rev	
Custom		1.0	
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GA-P81-D3

# DUAL BIOS

# MOSI For DMI RX Termination Voltage

12 N\_ICH\_SPI\_MOSI ← N\_ICH\_SPI\_MOSI NR10 8.2K/4/X  
12 N\_ICH\_SPI\_CS ← N\_ICH\_SPI\_CS NR9 8.2K/4/X  
18 -SPI\_HOLD\_M ← -SPI\_HOLD\_M NR3 1K/4/1  
18 -SPI\_HOLD\_B ← -SPI\_HOLD\_B NR11 1K/4/1

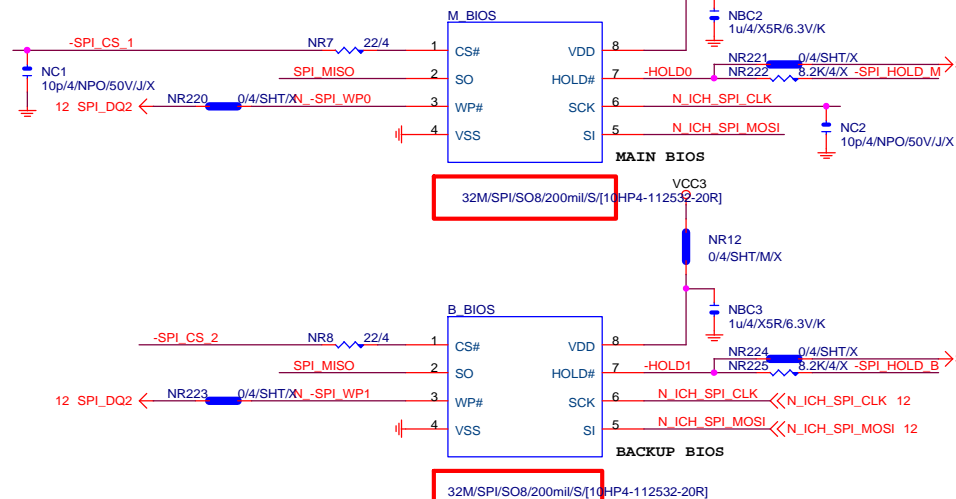
N\_-SPI\_WP1 NR2 8.2K/4/X  
N\_-SPI\_WP0 NR5 8.2K/4/X  
N\_ICH\_SPI\_MISO ← -HOLD0 NR235 1K/4/1/X  
N\_ICH\_SPI\_MISO ← -HOLD1 NR236 1K/4/1/X  
18 -SPI\_HOLD\_M ← -SPI\_HOLD\_M NR237 1K/4/1/X  
18 -SPI\_HOLD\_B ← -SPI\_HOLD\_B NR238 1K/4/1/X  
12 N\_ICH\_SPI\_MISO ← NR6 22/4 SPI\_MISO

BOOT DEVICE	GNT0	GNT1
LPC	0	0
PCI	0	1
NAND	1	0
SPI	1	1

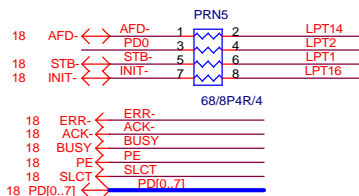
1 means floating  
0 means PD 1K

## 指定用DII

## 指定用DII

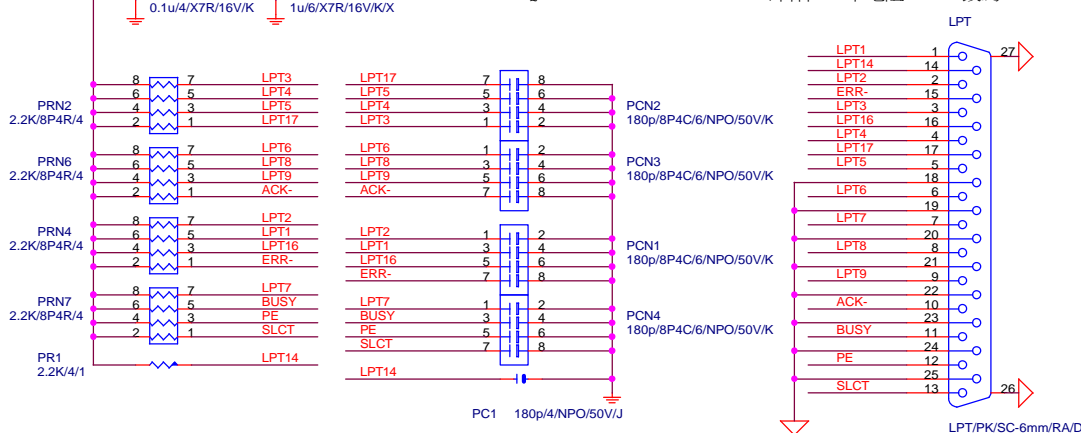


# LPT PORT

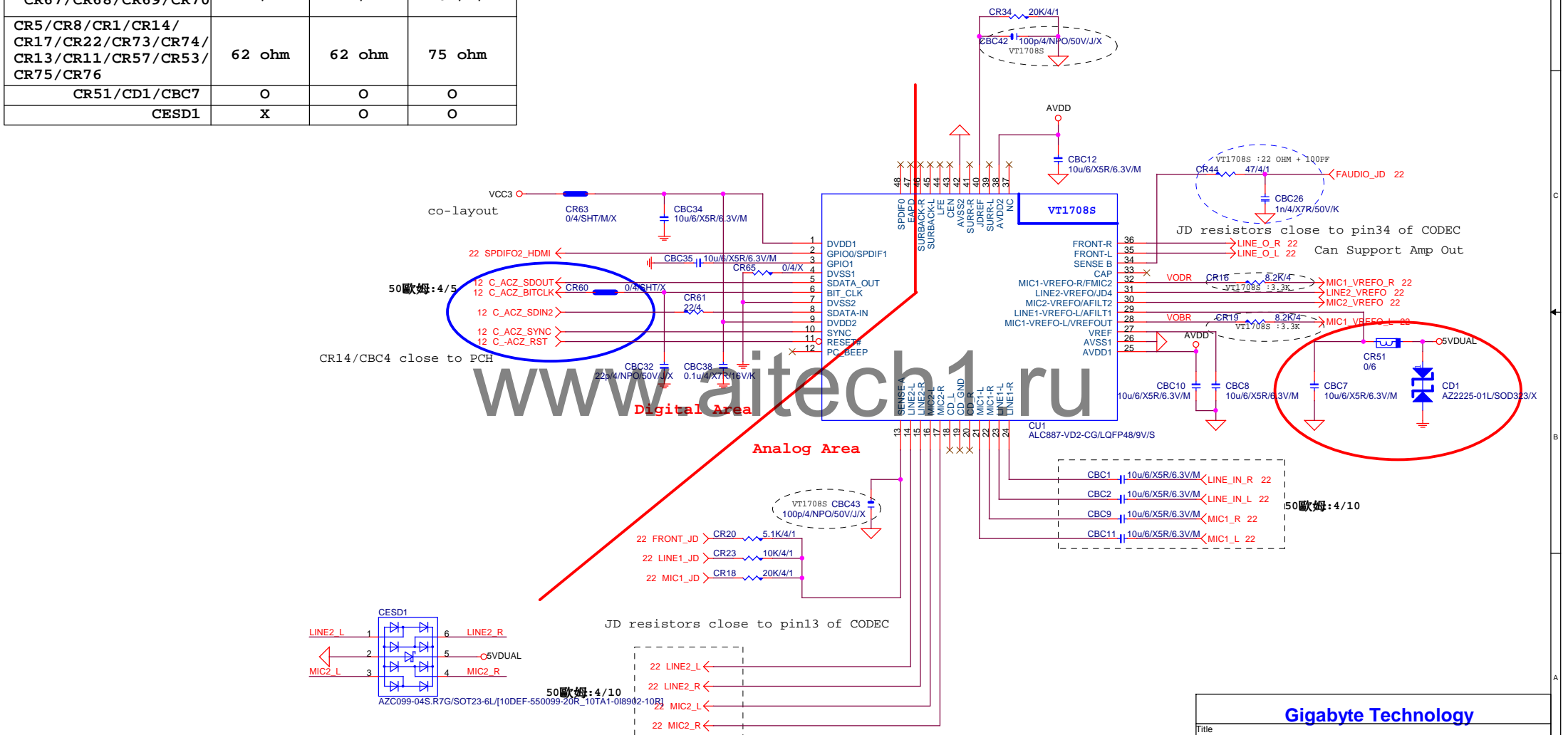


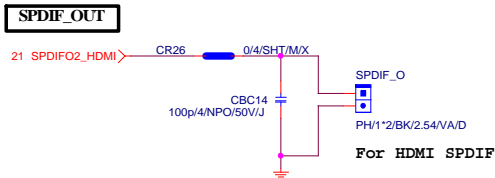
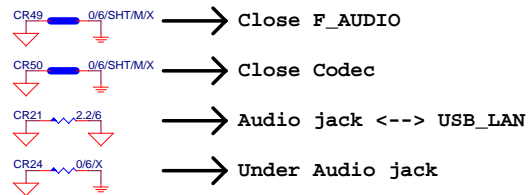
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R&D技術通報151 有使用PRINT PORT的  
MODEL, 需使用新料號: 10HP2-118728-72R (CHIP IT8728F/EX (GB) ITE/SMD  
QFP128 PRINTPORT SORTING) 料件。串電阻33 ohm改為68 ohm。

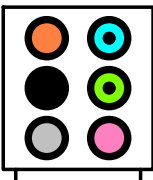


	ALC892	ALC887-VD2	VT1708S-CE
CR44/CBC26	47ohm+1nF	47ohm+1nF	22ohm+100P
CBC42/CBC43	X	X	100P/4
CR16/CR19 CR52/CR56/CR10/CR9	8.2K/4	8.2K/4	3.3K/4/1
CR6/CR7/CR58/CR54/ CR67/CR68/CR69/CR70	22K/4	22K/4	10K/4/1
CR5/CR8/CR1/CR14/ CR17/CR22/CR73/CR74/ CR13/CR11/CR57/CR53/ CR75/CR76	62 ohm	62 ohm	75 ohm
CR51/CD1/CBC7	O	O	O
CESD1	X	O	O

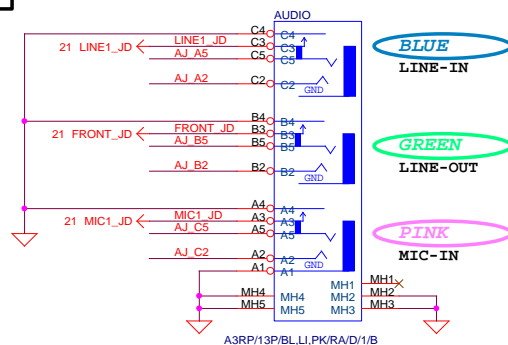




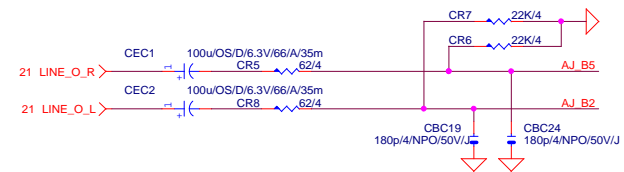
**AZALIA JACK**



**AZALIA JACK**

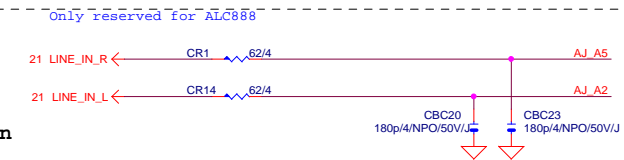


**LINE-OUT**

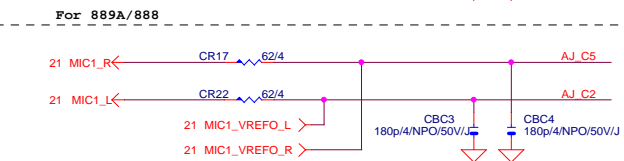


**LINE-IN**

Verify MIC function in LINE-in



**MIC-IN**

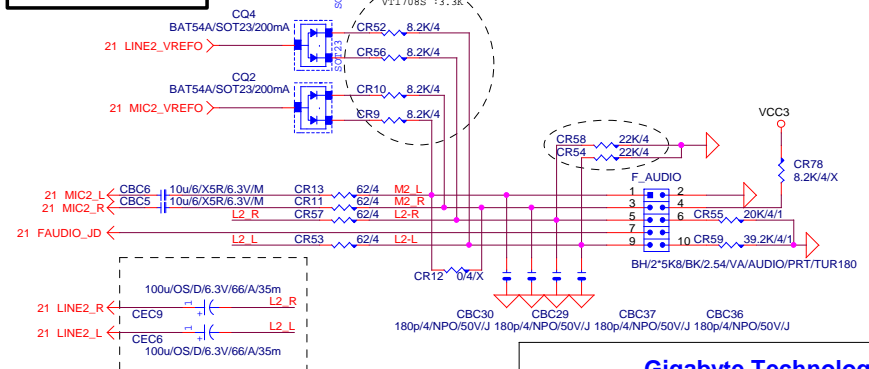


**SURROUND**

**CEN/LFE**

**SURRBACK**

**AZALIA FRONT PANEL**



**Gigabyte Technology**

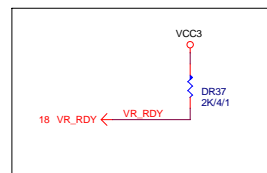
Title		
AUDIO JACK		
Size	Document Number	Rev
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R_PROG1 (Kohm)	3-Phase Iccmax(A)
24.9	105
28.7	114
<b>34.0</b>	<b>129</b>
42.2	144

R_PROG2 (Kohm)	Fsw(KHz)	VBOOT
<b>64.9</b>	<b>315</b>	<b>1.75</b>
73.2	315	1.70
80.6	315	1.65
90.9	315	0

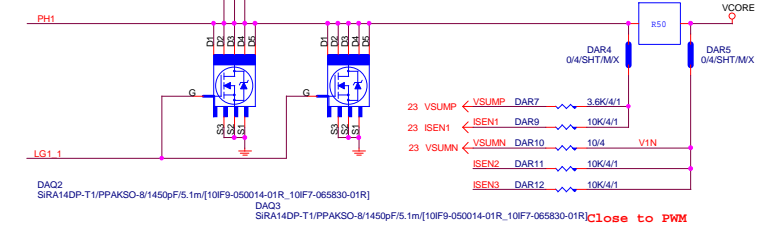
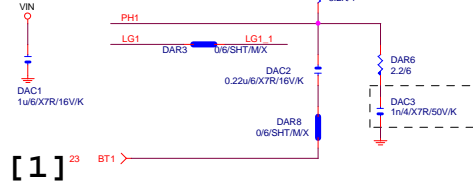
R_PROG3 (Kohm)	Fast Slew Rate (mV/us)
<b>3.24</b>	<b>12</b>
5.76	24
9.31	40
13.3	45



# PHASE 1



[1]



# PHASE 3



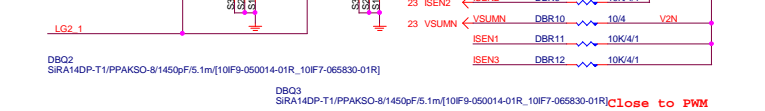
[3]



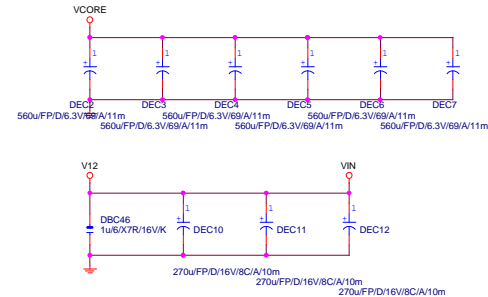
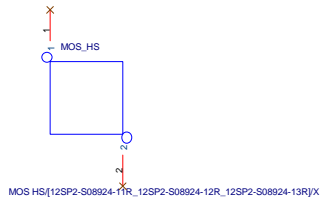
# PHASE 2



[2]

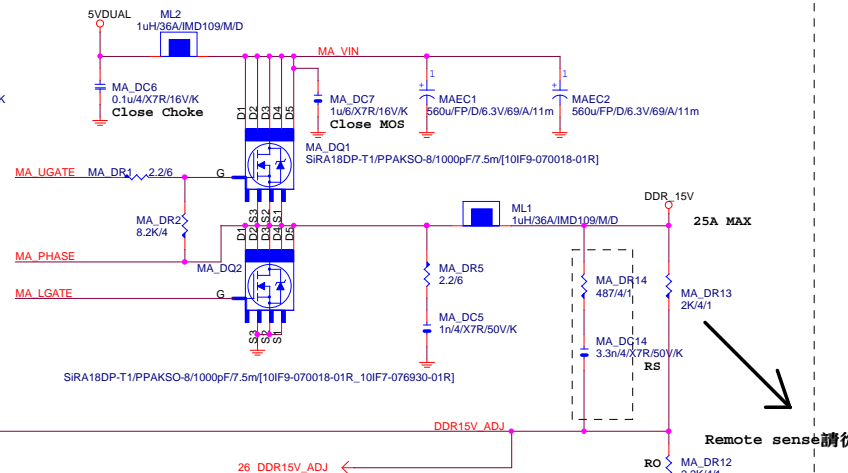
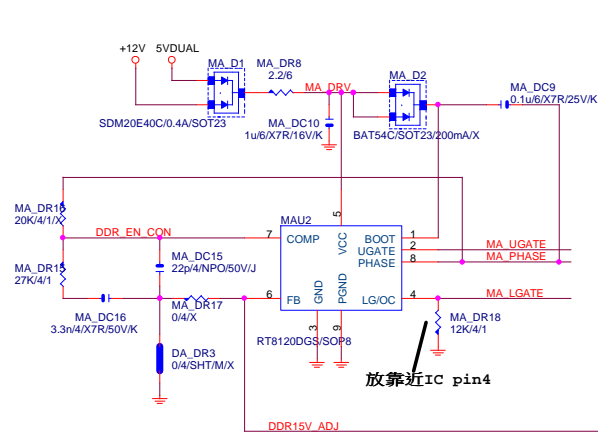


# MOSFET HEATSINK



<div>Gigabyte Technology</div>			
Title			
CPU CORE VR-2			
Size	Document Number		Rev
Custom	GA-P81-D3		1.0
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**DDR\_15V**



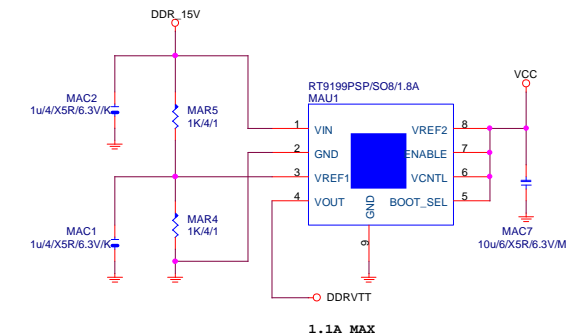
VIN=5V,VOUT=1.5V,IOUT=25A,PHASE=1  
IRMS=11.45A

560u/FP/D/6.3V/68/8m RIPPLE CURRENT=4.7A  
Coefficient=1.7(85°C),1(105°C)

VIN Ripple current=4.7X1.7=7.99A(85°C)  
-->故固態電容須2X7.99=15.98>11.45A

```
OCP:35.82A for Rds=6.7m for vishay@4.5V
OCP:72.727A for Rds=3.3m for renesas@10V
OCP:48A=Roset*Iocset / Rds(on)
      =12K*10uA / [5/5]
```

DDRVTT

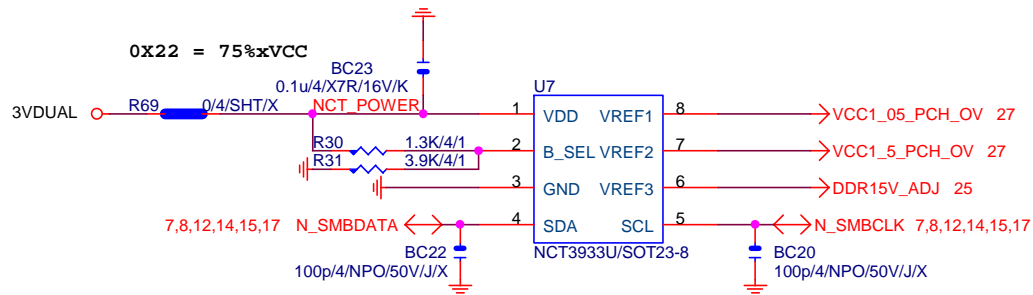


Remote sense請從最重的負載端點拉回

$$0.8 \cdot [1 + 2K / 2.2K] = 1.527V$$

Title			
<b>DDR15V / M3 POWER</b>			
Size	Document Number	Rev	
Custom	<b>GA-P81-D3</b>	<b>1.0</b>	
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OVER VOLTAGE



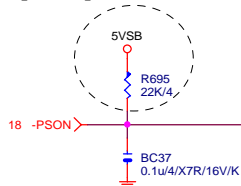
NCT3933	0X2A	0X20	0X22
VREF1	DDRVTT	VREF_DDRA_DQ	PCH Core
VREF2	VREF_DDRA_CA	N/A	VCC1_5_PCH
VREF3	VREF_DDRA_CA	VREF_DDRB_DQ	SMREF

Gigabyte Technology		
CPU CORE VR-2		
Title	Document Number	Rev
	GA-P81-D3	1.0
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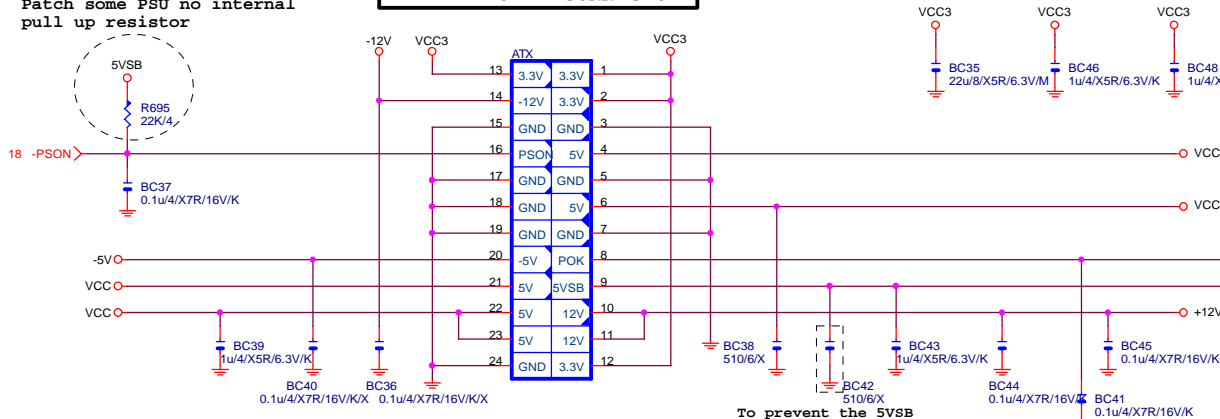




Patch some PSU no internal pull up resistor



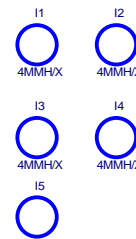
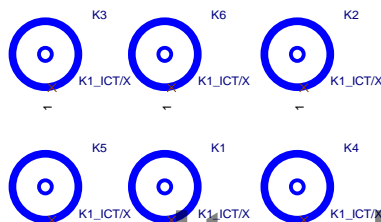
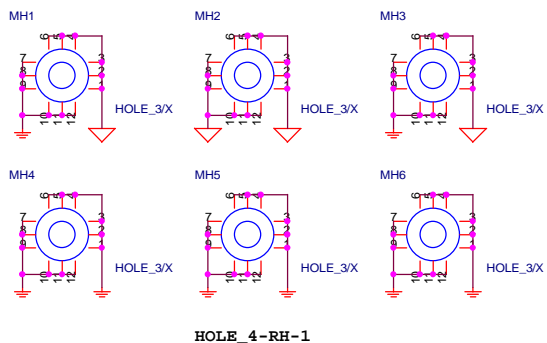
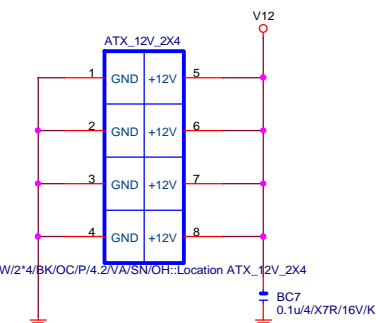
## ATXX24 POWER CONNECTOR



APW/2\*12/BK/VA/SN/2SHK/PA66

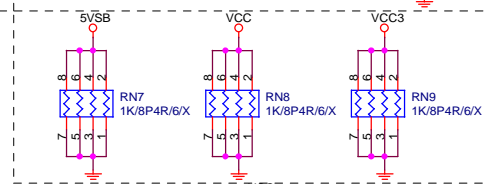
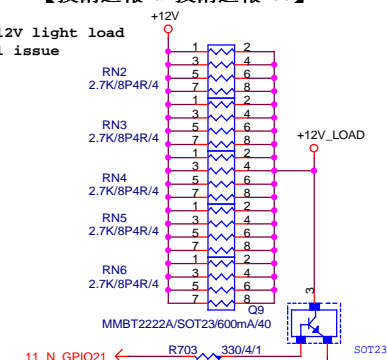
To prevent the 5VSB under loading when boot

## ATXX4 POWER CONNECTOR



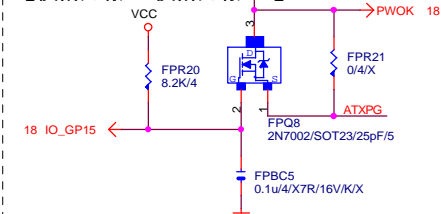
## 【技術通報R&D技術通報153】

To fix 12V light load abnormal issue



## PWOK PATCH

## 【技術通報R&D技術通報154】

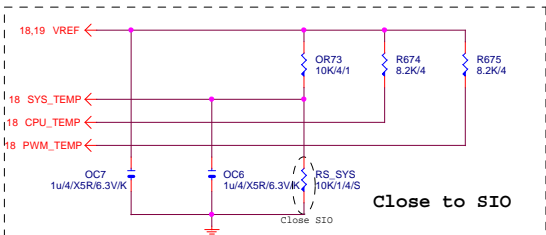


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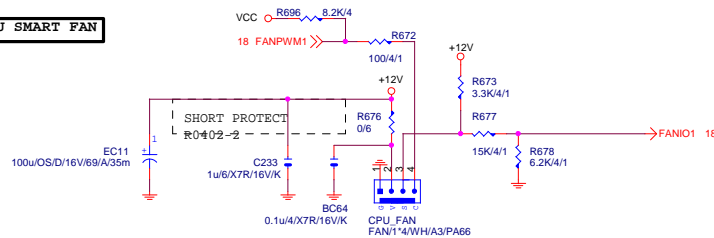
Title			ATX POWER CONNECTOR
Size	Document Number	Rev	1.0
Custom	GA-P81-D3		
Date:	Wednesday, March 05, 2014	Sheet	29 of 34



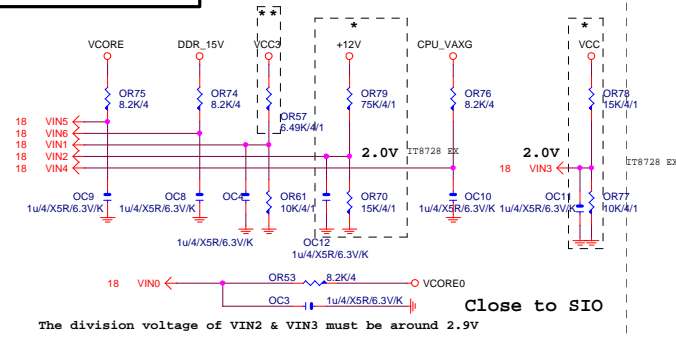
# TEMP H/W MONITOR



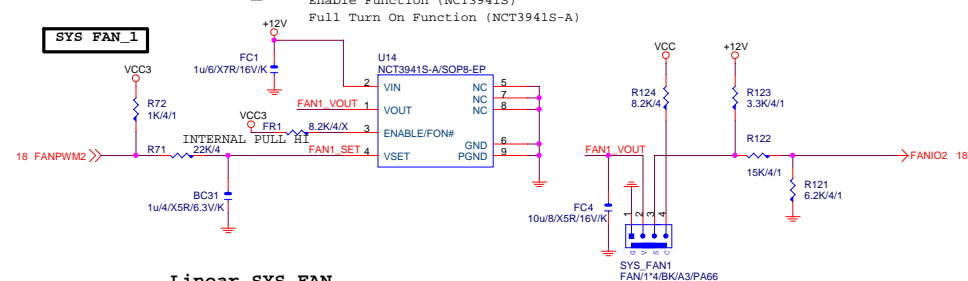
# CPU SMART FAN



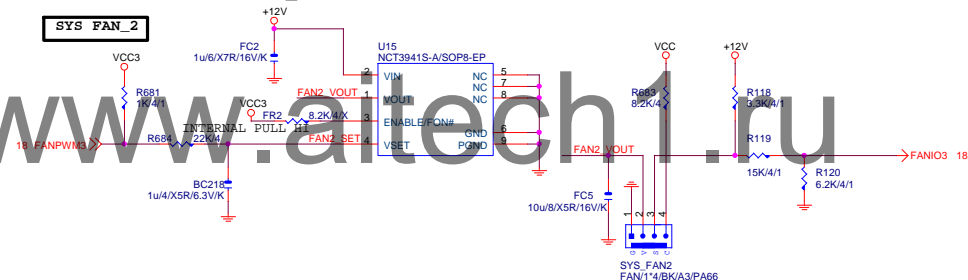
# VOLTAGE-- H/W MONITOR



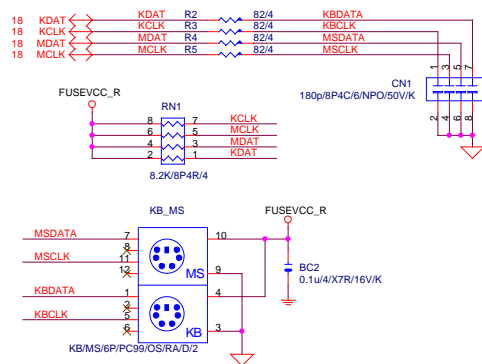
# Linear SYS\_FAN



# Linear SYS\_FAN



# KB/USB



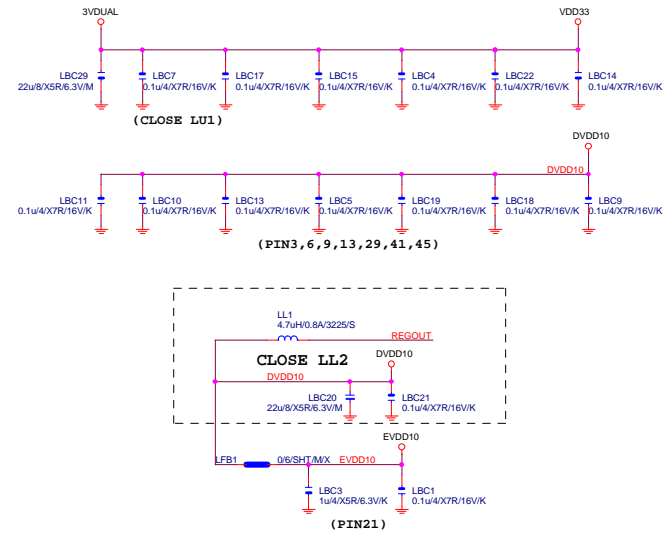
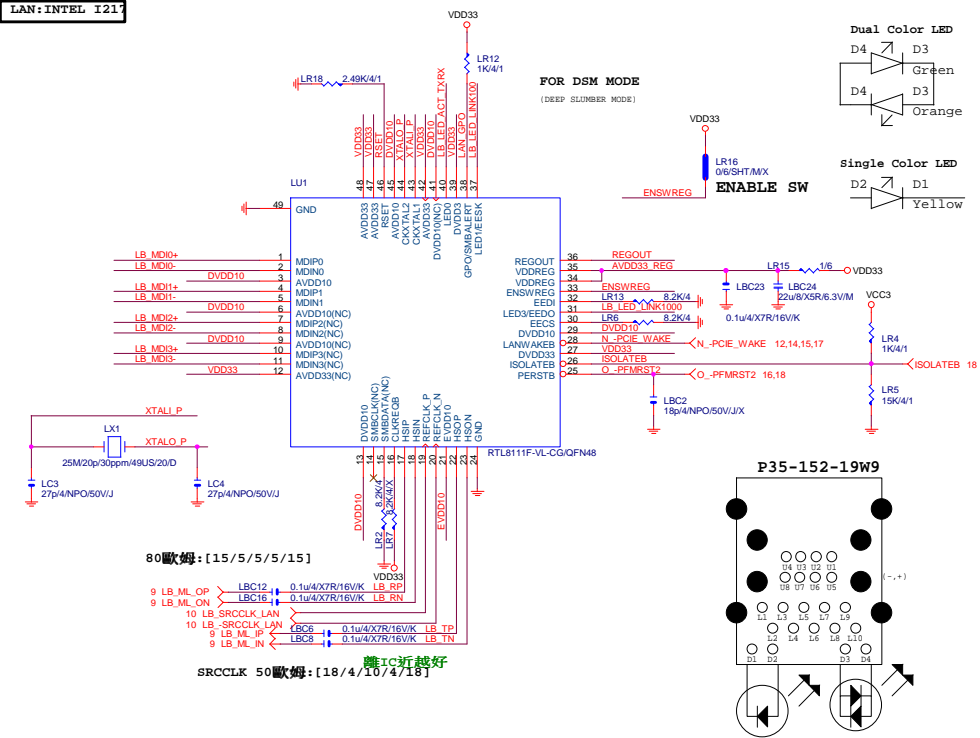
FOR FMI ONLY



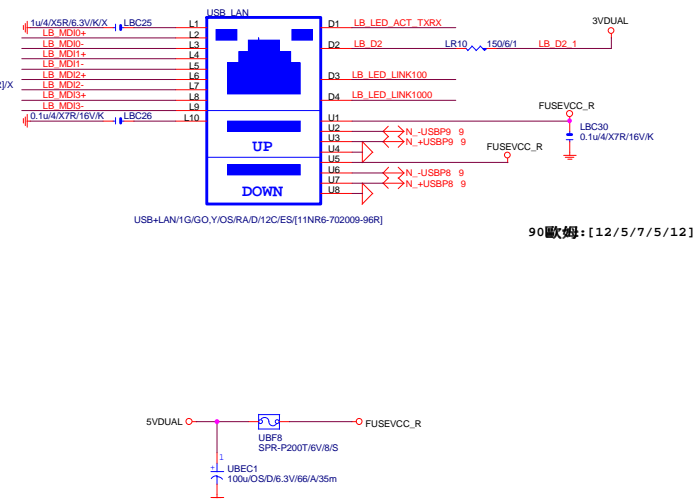
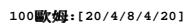
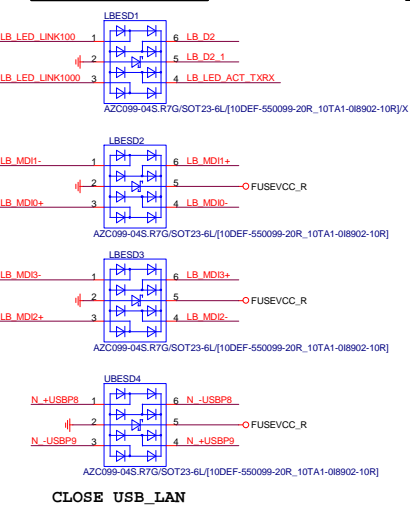
Gigabyte Technology

Title			HWM,KB/MS, FAN CTRL
Size	Document Number	Rev	
Custom	GA-P81-D3	1.0	
Date:	Wednesday, March 05, 2014	Sheet	30 of 34

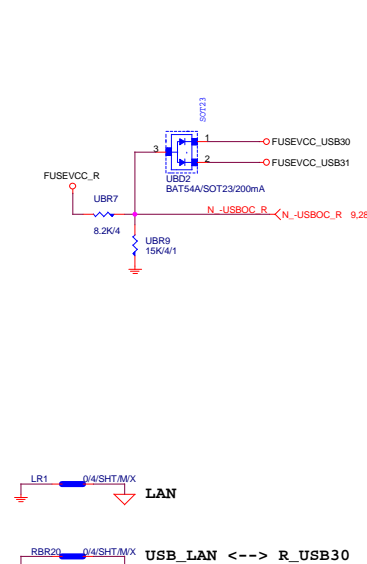
## LAN:INTEL I217



## USB30\_LAN CONNECTOR



## -USB0C\_R



www.aitech1.ru

Gigabyte Technology		
Title		
N/A		
Size	Document Number	Rev
Custom	GA-P81-D3	1.0
Date:	Wednesday, March 05, 2014	Sheet 32 of 34

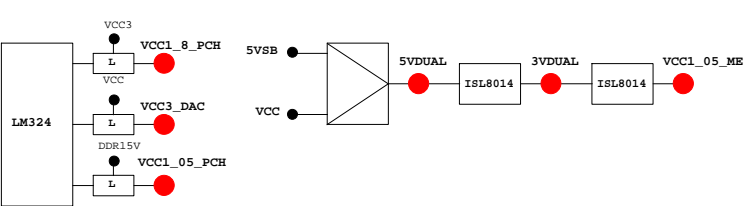
www.aitech1.ru

Gigabyte Technology		
Title		
N/A		
Size	Document Number	Rev
Custom	GA-P81-D3	1.0
Date:	Wednesday, March 05, 2014	Sheet 33 of 34

PIN	NAME	PWR	AFTER S4728	Default	USAGE	NOTE
GP0	MAIN	H-Z	GPI	GPIO0		N/A
GP1/TACH1	MAIN		GPI	GPIO1		N/A
GP2/PIRQE#	MAIN		GPI	-PIRQE		P/U 8.2K VCC3
GP3/PIRQF#	MAIN		GPI	-PIRQF		P/U 8.2K VCC3
GP4/PIRQG#	MAIN		GPI	-PIRQG		P/U 8.2K VCC3
GP5/PIRQH#	MAIN		GPI	-PIRQH		P/U 8.2K VCC3
GP6/TACH2	MAIN		GPI	PCIEX1 Detect		P/U 8.2K VCC3
GP7/TACH3	MAIN		GPI	GPIO7		P/U 8.2K VCC3
GP8	STBY	H	GPI	GPIO8		N/A
GP9/OC5#	STBY		NATIVE	USB OC5#		N/A
GP10/OC6#	STBY		NATIVE	USB OC6#		N/A
GP11/SMBALERT#	STBY		NATIVE	USB PWR protect		P/U 8.2K 3VDUAL
GP12	STBY	L	GPI	GPIO12		N/A
GP13	STBY	L	GPI	LPCPM#		P/U 8.2K 3VDUAL
GP14/OC7#	STBY		NATIVE	USB OC7#		N/A
GP15	STBY	L	GPI	GPIO15(TLS Enable)		P/U 8.2K 3VDUAL
GP16	MAIN		GPI	GPIO16		P/U 8.2K VCC3
GP17/TACH0	MAIN		GPI	GPIO17		P/U 8.2K VCC3
GP18	MAIN		GPI	Mobile Only		N/A
GP19	MAIN		GPI	GPIO19		P/U 8.2K VCC3
GP20	MAIN		GPI	GPIO20		P/U 8.2K VCC3
GP21	MAIN		GPI	GPIO21		P/U 8.2K VCC3
GP22	MAIN	H-Z	GPI	GPIO22		P/U 8.2K VCC3
GP23	MAIN		GPI	GPIO23		N/A
GP24	STBY	L	GPI	SKTOCC#		N/A
GP25	STBY			Mobile Only		N/A
GP26	STBY			Mobile Only		N/A
GP27	STBY	H	GPO	GPIO27		P/U 8.2K 3VDUAL
GP28	STBY	H	GPO	PWR LED		P/U 8.2K 3VDUAL
GP29	STBY	L	GPI	GPIO29		N/A
GP30	STBY	H-Z	GPI	Mobile Only		N/A
GP31	STBY	H-Z	GPI	Mobile Only		N/A
GP32	MAIN	H	GPO	N/A		N/A
GP33	MAIN	H	GPO	N/A		N/A
GP34	MAIN	H-Z	GPI	-PCI_STOP		P/U 8.2K VCC3
GP35	MAIN	L	GPO	-ACZ_DET		P/U 8.2K VCC3
GP36	MAIN		GPI	N/A		N/A
GP37	MAIN		GPI	N/A		N/A
GP38	MAIN	H-Z	GPI	PCIEX4 Detect		P/U 8.2K VCC3
GP39	MAIN	H-Z	GPI	GPIO39		P/U 8.2K VCC3
GP40	STBY		NATIVE	USB OC1#		N/A
GP41	STBY		NATIVE	USB OC2#		N/A
GP42	STBY		NATIVE	USB OC3#		N/A
GP43	STBY		NATIVE	USB OC4#		N/A
GP44	STBY	L	NATIVE	GPIO44		P/U 8.2K 3VDUAL
GP45	STBY		NATIVE	GPIO45		P/U 8.2K 3VDUAL
GP46	STBY	L	NATIVE	GPIO46		P/U 8.2K 3VDUAL
GP47	STBY			Mobile Only		N/A
GP48	MAIN	H-Z	IN	GPIO48		P/U 8.2K 3VDUAL
GP49	MAIN	H-Z	IN	GPIO49		P/U 8.2K 3VDUAL
GP50	MAIN		NATIVE	-REQ1		P/U 2.2K VCC
GP51	MAIN	H	NATIVE	-GNT1		N/A
GP52	MAIN		NATIVE	-REQ2		P/U 2.2K VCC
GP53	MAIN	H	NATIVE	-GNT2		N/A
GP54	MAIN		NATIVE	-REQ3		P/U 2.2K VCC
GP55	MAIN	H	NATIVE	-GNT3		N/A
GP56	STBY		NATIVE	Mobile Only		N/A
GP57	STBY	H-Z	IN	VCORE_OV1		P/U 8.2K 3VDUAL
GP58	STBY	H-Z	NATIVE	F_USB_OC		P/U 8.2K 3VDUAL
GP59	STBY		NATIVE	USB_OC0#		N/A
GP60	STBY	H-Z	NATIVE	N/A(Reverse)		P/U 8.2K 3VDUAL
GP61	STBY	L	NATIVE	-SUSTAT		N/A
GP62	STBY	L	NATIVE	SUSCLK		N/A
GP63	STBY	L	NATIVE	GPIO63		N/A
GP64	MAIN	L	NATIVE	CLKOUTFLEX0		N/A
GP65	MAIN	L	NATIVE	CLKOUTFLEX1		N/A
GP66	MAIN	L	NATIVE	CLKOUTFLEX2		N/A
GP67	MAIN	L	NATIVE	CLKOUTFLEX3		N/A
GP72	STBY	H-Z	NATIVE	VCORE_OV4		P/U 8.2K 3VDUAL
GP73	STBY			Mobile Only		N/A
GP74	STBY	H-Z	NATIVE	1_05V_OV2		P/U 8.2K 3VDUAL
GP75	STBY	H-Z	NATIVE	N/A(Reverse)		P/U 8.2K 3VDUAL

PIN NAME	USAGE	NOTE
SVC/PECI_RQT/GP14	-PECI_REQ	
PWROK1/GP13	PWROK1/ITE_PWROK	
KRST#/GP62	-KBRST	
SO/GP50	-ICH_SPI_CS	
IRTX/GP47/CE2_N/JP7	CEB_N	
GP46/IRRX	-LAN2_DSM	
PSION#/GP42	-PSON	
PWROK2#/GP41	PECI_CTL	
PCIRST3#/GP10/VDIMM_STR_EN	-PCIE_RST	
RSMRST#CIRRXL1/GP55	-RSMRST	
PME#/GP54	-LPCPME	
PD5/GP75/BUSS00	N/A	

PIN NAME	USAGE	NOTE
FAN_TAC2/GP52	FANIO2	
FAN_TAC3/GP37	FANIO3	
VIDO3/FAN_TAC4/GP25/DSR2#	FANIO4	
FAN_CTL2/GP51	FANPWM2	
FAN_CTL3/GP36	FANPWM3	
VID4/GP34	BEEP-	
VID3/GP33	TURBO1	
VID2/GP32	TURBO0	
VCORE_GOOD/VID6/GP63	CPUT_LED1_C	
VID5/GP35	CPUT_LED2_C	
VID1/GP31	CPUT_LED3_C	
VID0/GP30	-LAN1_DSM	NBT_LED1_C
SLCT/GP80	CPU_LED1_C	
PE/GP81	CPU_LED2_C	
BUSY/GP82	CPU_LED3_C	
PD3/GP73/BUSSI1	SB_LED1_C	
PD4/GP74/BUSSI2	SB_LED2_C	
VCORE_EN/VID7/GP64	IT_GP64	SB_LED3_C
PD0/GP70	NB_LED1_C	
PD1/GP71	NB_LED2_C	
PD2/GP72/BUSSI0	NB_LED3_C	
GP22/SCK	LOW_PWR_1	
VIDO5/GP27/SIN2	LOW_PWR_2	
PCIRST2#/GP11	-PFMRST1	
PCIRST1#/GP12	-PFMRST2	
3VSBSW#/GP40	CSI_F0	BSEL166_1
SUSC#/GP53	CSI_F1	BSEL166_2
GP23/SI	BSEL166_3/CSISBSL	
VIDO0/GP20/CTS2#	CPUT_LED1_C	BSEL166_4
GP65/VDDA_EN/GB_01	MB_ID2	
PD6/GP76/BUSSO1	MB_ID3	
PD7/GP77/BUSSO2	MB_ID4	
AFD#/GP86/SMBC_R	2X PIN	FST_2X8
INIT#/GP85/SMBD_M	SEC_2x8	GTLREF_AD2
ACK#/GP83	DDR_LED1_C	
VIDO1/GP21/DCD2#	DDR_LED2_C	
STB#/GP87/SMBC_M	DDR_LED3_C	
PWRON#GP44	VCORE_OV1	
PANSWH#/GP43	PWRBTSW	
KDAT/GP61	-PWRBTSW	
KCLK/GP60	KDAT	
MDAT/GP57	KCLK	
MACL/GP56	MDAT	
GP66/VLDT_EN/GB_02	NBT_LED1_C	MCLK
SVD/PCIRSTIN#/CIRTX/GP15	PWM2_CR	
KDAT/GP61	PWM2_CR	
GP67/CPU_PG/GB_03	EN_LOADLINE	IT_GP67/-EN_PWM2
SLIN#/GP84/SMBD_R	-EN_PWM2	
PS1_L/FAN_CLT5/CIRRX2/GP16	-THERM	
VIDO4/GP26/SOUT2	DDR18V_PH2_EN	
VIDO2/FAN_TAC5/GP24/DSR2#	DDR18V_LED	
VIDO6/GP17/RI2#	1_1V_PH_EN	
VIDO7/JP6/DTR2#	JP6	
PD5/GP75/BUSS00	SB_LED3_C	



The diagram illustrates a system architecture with the following components and connections:

- CPU\_VTT** and **VCORE** are connected to the **CPU SOCKET** via a dashed line.
- MOSFET** and **CHOKE** are connected to the **CPU SOCKET** via a dashed line.
- PCH** is connected to the **CPU SOCKET** via a dashed line.
- VAXG** is connected to the **CPU SOCKET** via a dashed line.
- P-PAK** is connected to the **CPU SOCKET** via a dashed line.
- The **CPU SOCKET** is connected to the **CPU\_VTT** and **VCORE** via a dashed line.
- The **CPU SOCKET** is connected to the **MOSFET** and **CHOKE** via a dashed line.
- The **CPU SOCKET** is connected to the **PCH** via a dashed line.
- The **CPU SOCKET** is connected to the **VAXG** via a dashed line.
- The **CPU SOCKET** is connected to the **P-PAK** via a dashed line.

Detailed description of the diagram components and connections:

- CPU\_VTT** and **VCORE** are connected to the **CPU SOCKET** via a dashed line.
- MOSFET** and **CHOKE** are connected to the **CPU SOCKET** via a dashed line.
- PCH** is connected to the **CPU SOCKET** via a dashed line.
- VAXG** is connected to the **CPU SOCKET** via a dashed line.
- P-PAK** is connected to the **CPU SOCKET** via a dashed line.
- The **CPU SOCKET** is connected to the **CPU\_VTT** and **VCORE** via a dashed line.
- The **CPU SOCKET** is connected to the **MOSFET** and **CHOKE** via a dashed line.
- The **CPU SOCKET** is connected to the **PCH** via a dashed line.
- The **CPU SOCKET** is connected to the **VAXG** via a dashed line.
- The **CPU SOCKET** is connected to the **P-PAK** via a dashed line.

線路圖名稱	BIOS選項
Vcore	CPU Vcore
CPU_VTT	CPU Termination
CPU_VAXG	CPU Graphic Core
VCC1_8_PCH	CPU PLL
VCC1_05_PCH	PCH core
3VDUAL	3VDUAL
DDR15V	DRAM voltage
DDRVTT	DRAM Termination
VREF_CA_A/VREF_CA_B	DRAM Address Ref
VREF_DQ_A/VREF_DQ_B	DRAM Data Ref

Z77-D3H :  
PCH :  
12SP2-S05511-01R/02R/03R  
MOSFET :  
12SP2-S08924-01R/02R/03R

	3 pin FAN control	4 pin FAN control	FAN speed	Controller
CPU FAN	FANPWM1	FANPWM3	FANIO1	IT8720
	ICH_FAN_PWM2	ICH_FAN_PWM0	ICH_FAN_TACH0	PCH
SYS FAN	FANPWM2	N/A	FANIO2	IT8720
	ICH_FAN_PWM1	N/A	ICH_FAN_TACH1	PCH
PWR FAN	N/A	N/A	FANIO3	IT8720
			ICH_FAN_TACH2	PCH